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SOFTWARE MEMO FOR THE MULTIMODE SONAR CONSOLE DISPLAY SYSTEM. V--ETC(U)
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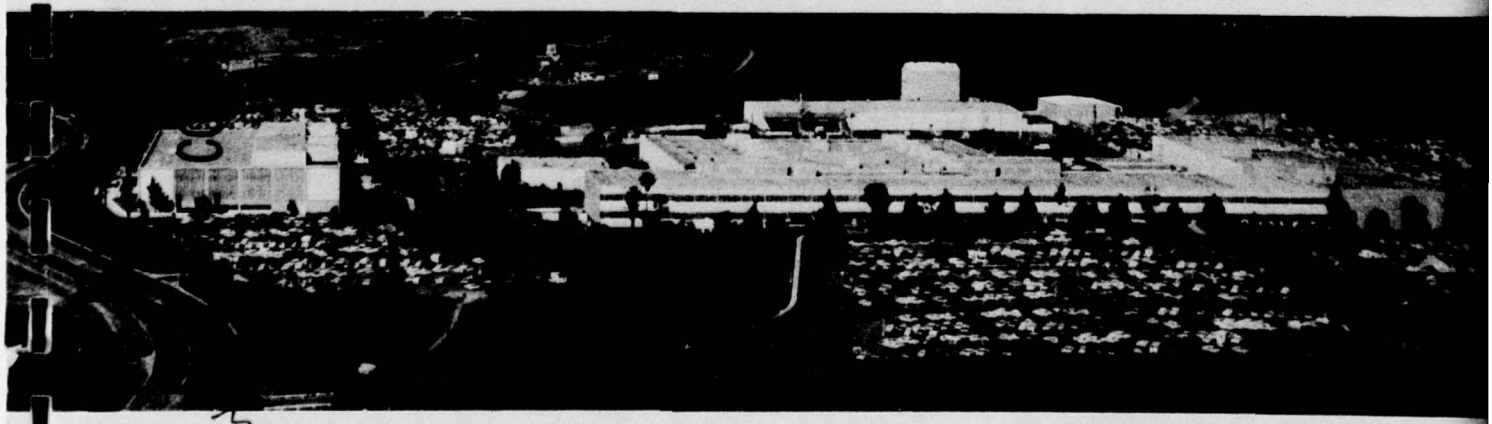
HUGHES
HUGHES AIRCRAFT COMPANY
FULLERTON, CALIFORNIA

MOST Project -3

VOLUME I - OPERATIONAL PROGRAMMING

SOFTWARE MEMO FOR THE MULTIMODE SONAR CONSOLE DISPLAY SYSTEM

9 AUGUST 1968
N00123-67-C-0833



SOFTWARE MEMO FOR THE MULTIMODE SONAR CONSOLE DISPLAY SYSTEM

Volume I – Operational Programming

Submitted to
Navy Undersea Warfare Center
San Diego, California

by

Hughes Aircraft Company
Hughes-Fullerton
Fullerton, California

FR-68-11-653
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FOREWORD

This report, submitted to the Navy Undersea Warfare Center San Diego, by Hughes Aircraft Company, is a contractually required document under Contract No. N00123-67-C-0833. The report describes the operations of the Multi-Mode Sonar Console and Passive Data Memory Unit from the viewpoint of the computer programmer. Instruction and data-word formats for each of the equipments are described, as are the actions that occur in response to the instructions and data words. For convenience in handling, the document is divided into two volumes: Volume I describes operational programming and Volume II describes diagnostic programming.

In the preparation of this report, it has been assumed that the reader is familiar with the UNIVAC 1230 computer, with logical operations, and with the basic principles of computer-controlled display generation. The information in this report will permit the reader to write valid programs for generating versatile sonar displays.

CONTENTS

SUMMARY

SUMMARY OF MMSC DISPLAY SYSTEM

The MMSC display system combines a group of stored-program, general-purpose Multi-Mode Sonar Consoles with a Passive Data Memory Unit for interface with a UNIVAC computer to provide for storage and display of sonar data.

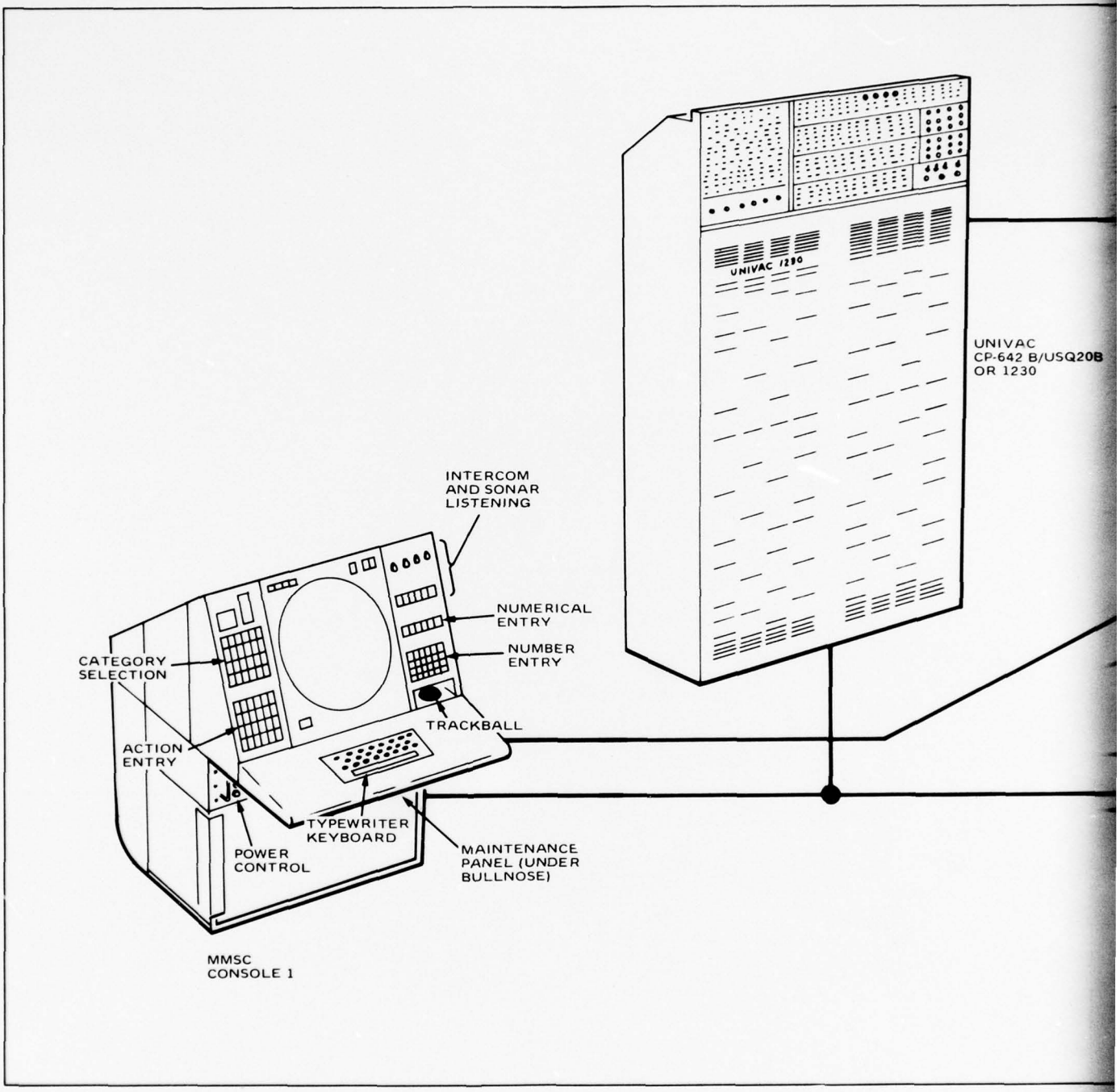
The Multi-Mode Sonar Console display-system consists of one to seven Multi-Mode Sonar Consoles (MMSC's) and a single Passive Data Memory Unit (PDMU). The MMSC display system provides versatile display capability for computer-aided sonar systems. The MMSC's and PDMU will interface with either the militarized UNIVAC CP-642B/USQ-20B or the UNIVAC 1230 computer. (See the facing figure.) The MMSC display system does not interface directly with the sonar sensor sub-system. All active and passive sonar data are assembled, formatted, and transmitted to the MMSC display-system by the computer.

The design of the MMSC's will allow seven consoles or less to time-share a single, fast-interface, input/output channel of the computer. The PDMU operates on its own fast interface channel.

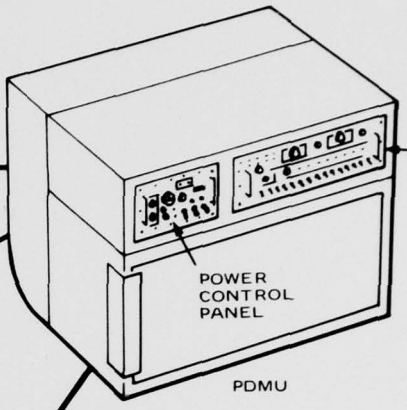
MMSC Features – The MMSC is a stored-program general-purpose sonar console. The program and display data are stored in the console's 8K, 36-bit word, random-access memory. Information is displayed on the CRT by cycling through the memory under control of the stored program. A selectable frame rate of either 35 or 50 Hz permits a steady state, non-flickering display. Features of the MMSC are summarized on the figure.

PDMU Features – The PDMU provides BTR display data in a variety of formats for the MMSC consoles. In performing this function the PDMU is required to store passive sonar data transmitted by the computer. The passive data, along with a limited number of program words, are stored in an 8K, 36-bit word, random access memory. The program words allow the BTR raster to be displayed in up to 15 bands with variable band spacing. In addition, the program words allow optimizing the data rate between the computer and PDMU. The computer may instruct the PDMU to format the passive data in one of seven formats which define the number of beams to be displayed and their widths. The format determines the required pulse trains to be transmitted by the PDMU to the consoles. The PDMU can transmit raster data in parallel to up to seven MMSC's.

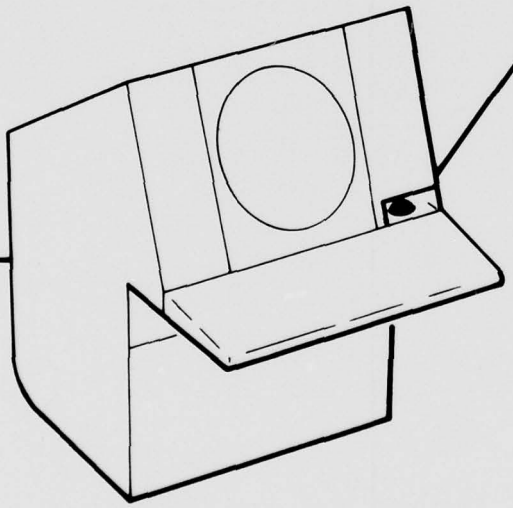
Programming – Two essentially different types of programming exist within the MMSC display-system. One group of instructions is used in the exchange of information between the computer and MMSC display-system. This type of communication initiates a direct action in either the computer or MMSC display-system (e.g., a command transmitted by the computer to a particular MMSC to load the next block of transmitted words into its memory). This type of programming is similar for both the MMSC and PDMU and is presented in Section 1. In the second group, the instructions are initially data words which are transmitted by the computer to be loaded into an MMSC's or PDMU's memory. However, when these words are read out of memory during the normal course of operation, they become instructions which directly control the display on the CRT in the case of the MMSC, or raster generation in the case of the PDMU. This second group of instructions is presented in two sections as MMSC programming (Section 3) and PDMU programming (Section 4).


UNIVAC 1230
UNIVAC
CP-642 B/USQ20B
OR 1230
INTERCOM
AND SONAR
LISTENING
NUMERICAL
ENTRY
NUMBER
ENTRY
CATEGORY
SELECTION
TRACKBALL
ACTION
ENTRY
TYPEWRITER
KEYBOARD
POWER
CONTROL
MAINTENANCE
PANEL (UNDER
BULLNOSE)
MMSC
CONSOLE 1

UNIVAC
CP-642 B/USQ20B
OR 1230



PDMU



MMSC
CONSOLE 7

FEATURES OF THE MMSC

- PROGRAMMABLE SYMBOL SHAPES
- ALPHANUMERIC TYPEWRITER DISPLAY
- BTR DISPLAY (WHEN USED WITH A PDMU)
- TIME COMPRESSED PING HISTORY DISPLA
- LINE DISPLAY (NEARLY CONSTANT WRITE
- SECTOR EXPANSION
- COMPUTER CONTROLLED LABELS FOR AL PUSHBUTTONS, ACTION ENTRY PUSHBUT PUSHBUTTONS
- COMPUTER INITIATED ON-LINE TESTING
- 7 INTENSITY LEVELS

PDMU FEATURES

- 7 FORMATS FOR NUMBER OF BEAMS AND
- 7 BRIGHTNESS LEVELS FOR SIGNAL STRE
- 15 BANDS TO ALLOW DISPLAY OF PASSIV DIFFERENT TIME CONSTANTS
- VARIABLE BAND WIDTH SPACING
- PARALLEL OUTPUT FOR UP TO 7 MMSC
- COMPUTER INITIATED ON-LINE TESTING

Configuration of the Multi-Mode Sonar Console Display-System. Features of the MMSC and P

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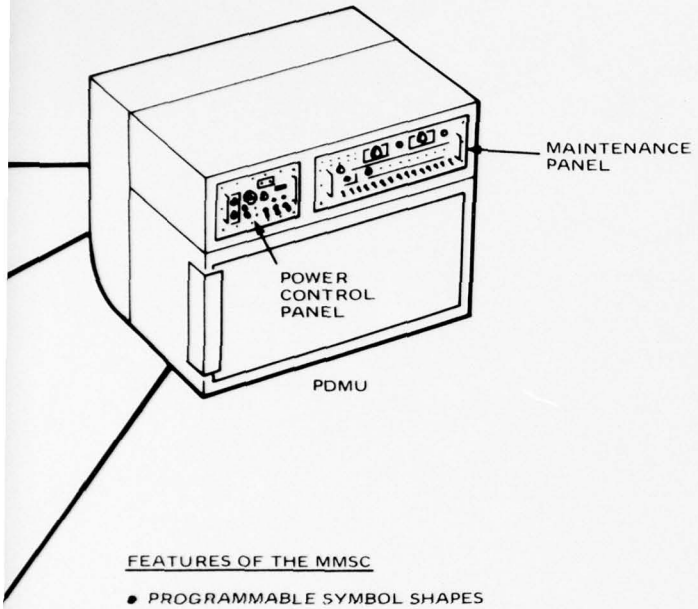

FEATURES OF THE MMSC

- PROGRAMMABLE SYMBOL SHAPES
- ALPHANUMERIC TYPEWRITER DISPLAY
- BTR DISPLAY (WHEN USED WITH A PDMU)
- TIME COMPRESSED PING HISTORY DISPLAY
- LINE DISPLAY (NEARLY CONSTANT WRITING RATE FOR ALL LINES)
- SECTOR EXPANSION
- COMPUTER CONTROLLED LABELS FOR ALERTS, CATEGORY SELECTION PUSHBUTTONS, ACTION ENTRY PUSHBUTTONS, AND NUMERICAL ENTRY PUSHBUTTONS
- COMPUTER INITIATED ON-LINE TESTING CAPABILITY
- 7 INTENSITY LEVELS

PDMU FEATURES

- 7 FORMATS FOR NUMBER OF BEAMS AND WIDTH
- 7 BRIGHTNESS LEVELS FOR SIGNAL STRENGTH
- 15 BANDS TO ALLOW DISPLAY OF PASSIVE DATA WITH DIFFERENT TIME CONSTANTS
- VARIABLE BAND WIDTH SPACING
- PARALLEL OUTPUT FOR UP TO 7 MMSC'S
- COMPUTER INITIATED ON-LINE TESTING CAPABILITY

ay-System. Features of the MMSC and PDMU are listed in the figure.

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SECTION 1
COMPUTER/DISPLAY SYSTEM COMMUNICATIONS

FUNCTIONAL ORGANIZATION FOR COMMUNICATIONS

Similar Input/Output units are contained in both the MMSC and PDMU to enable communications with the computer.

Each MMSC and PDMU contains an Input/Output (I/O) unit which acts as a buffer for communications between the computer and the equipment containing the I/O unit. The I/O unit for the MMSC and PDMU are essentially identical. A block diagram of the functions used in communications between the computer and the MMSC or the PDMU is shown in the facing figure. A brief discription of these functions follows.

Input Logic – The Input Logic consists of three functional logic groups: Input Source Selection Gates, Assembly Logic, and the Input Load Control Logic. The Input Source Selection Gates are used to select either the 30-bit lines from the computer or the 30-bit switches from the maintenance panel. The source selection is controlled by the "On-Line/Off-Line" switch on the maintenance panel. The Assembly Logic is used to convert two 30-bit acknowledge words from the computer into a 36 bit word for storage in the memory. The Input Load Control Logic detects word types, external function, acknowledge word 1 or acknowledge word 2, and generates control and timing signals.

Input Register – The Input Register provides temporary buffer storage for assembled acknowledge words or external function words.

Memory Load/Unload Control – The memory load flip-flop and memory unload flip-flop are contained in the Memory Load/Unload Control. These flip-flops are set and reset by external function commands, thus storing the load and unload commands. A PDMU or MMSC is capable of full duplex operation, thus both flip-flops may be set at the same time. The Memory Load/Unload Control logic generates timing signals that control memory operation.

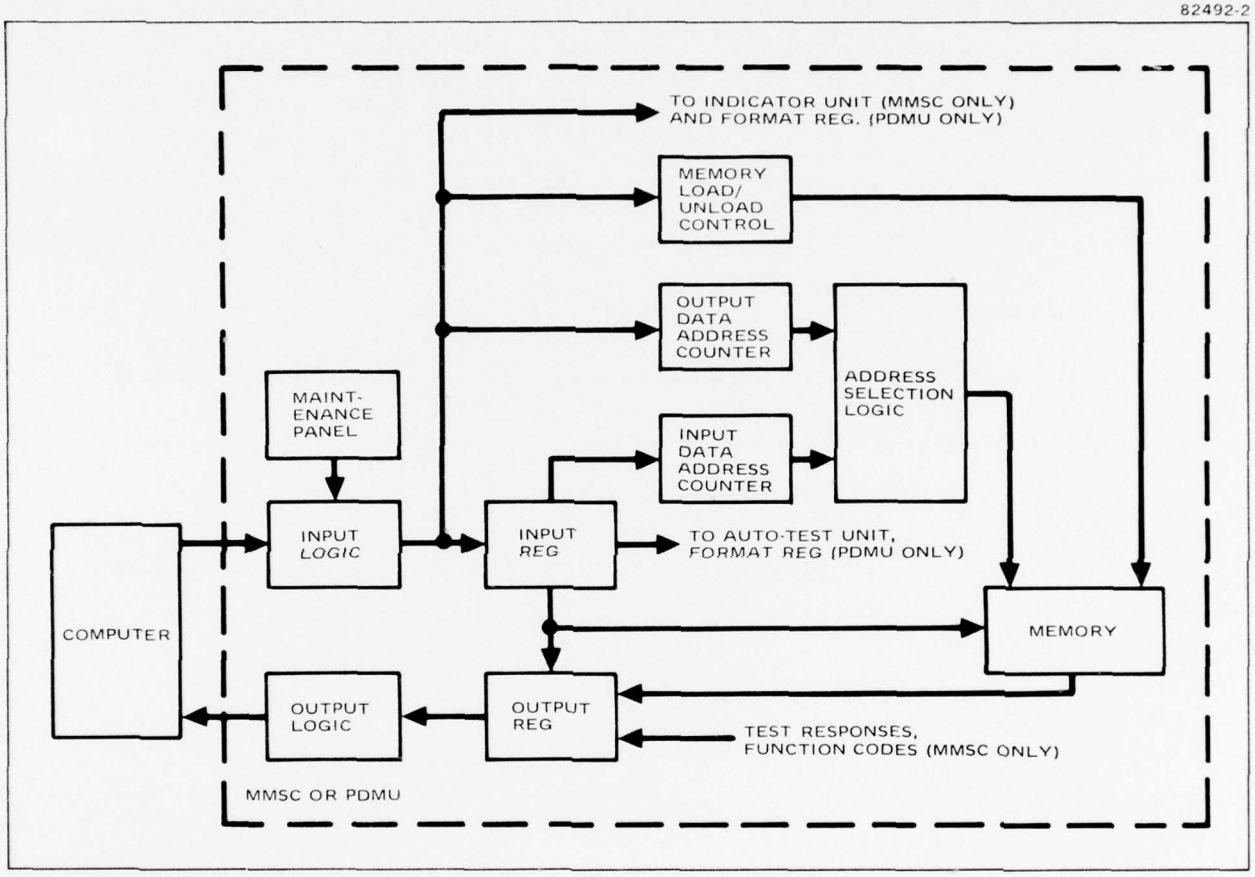
Input Data Address Counter – The Input Data Address Counter is preset with an address contained in word 1 of an output acknowledge word pair. This address specifies the location in memory in which the 36-bit word in the input register is to be stored. The counter is only activated after the MMSC or PDMU receives a memory load start external function. The counter has an increment mode that may be used by setting to zero, bit 13 of each acknowledge word 1.

Output Data Address Counter – This counter is used after receipt of a memory unload start external function to address words in the memory for return to the computer. It is preset to the start address by the memory unload start external function.

Address Selection Logic – The Address Selection Logic allows the address lines to the memory to be time shared by a number of sources. There are other sources than the two indicated in the drawing but they are not used in computer communications.

Output Register – The Output Register is a 36-bit buffer storage that stores memory words, auto-test responses, or function codes. One memory word is transmitted to the computer by two input request words. The Output Register isolates the memory from the computer input channel.

Output Logic – The Output Logic consists of the disassembly logic gates and the output mode control logic. The disassembly logic converts the 36-bit memory word into two 30-bit input request words. The mode control logic sets the interrupt and input request lines to the computer and generates internal timing signals.

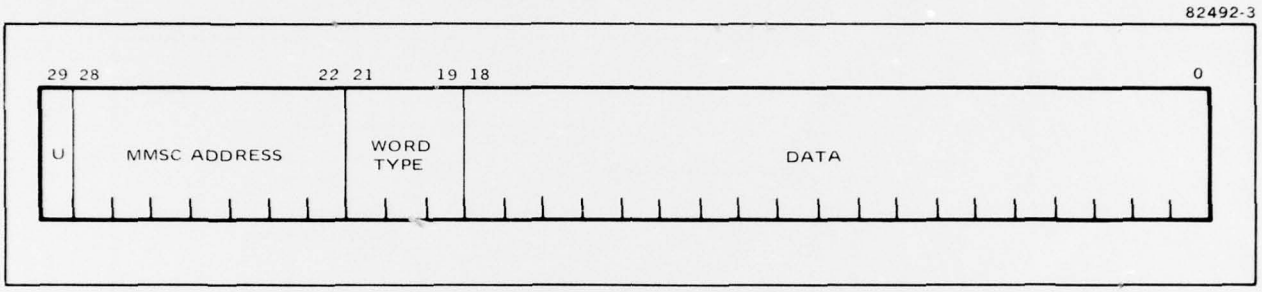


Functions Used in Communications with the Computer. Input/Output units in the MMSC and PDMU are essentially identical

FORMAT FOR EXTERNAL FUNCTION WORDS

External function words control memory loading/unloading, initiate auto-tests, set panel indicators in an MMSC, and select the passive display format in the PDMU.

General Description of External Function Word – External function words are sent from the computer to an MMSC or PDMU and used to load and unload the memory, initiate auto-tests, set panel indicators in an MMSC, and define the passive display format in a PDMU. External function words can be sent when the external function request line to the computer is set. Use of the forced external function by the computer may cause loss of the data in the MMSC's or PDMU's Input Register.



General Format of External Function Word

Bits 0 - 18 — Contains auxiliary data which is loaded into bits 0 - 18 of the input register.

Bits 19 - 21 — Word type – defines the operation to be performed.

Codes				Definition
21	20	19	Octal	
0	0	0	0	not used
0	0	1	1	memory load start
0	1	0	2	memory load stop
0	1	1	3	memory unload start
1	0	0	4	memory unload stop
1	0	1	5	indicator (MMSC) passive format (PDMU)
1	1	0	6	test stimulus
1	1	1	7	not used

Bit 22-28 – These bits are unused in the PDMU. In the MMSC, they specify the console address. The operation defined by the word type will be performed at the console(s) whose corresponsing address bit is set. Any number of address bits may be set simultaneously.

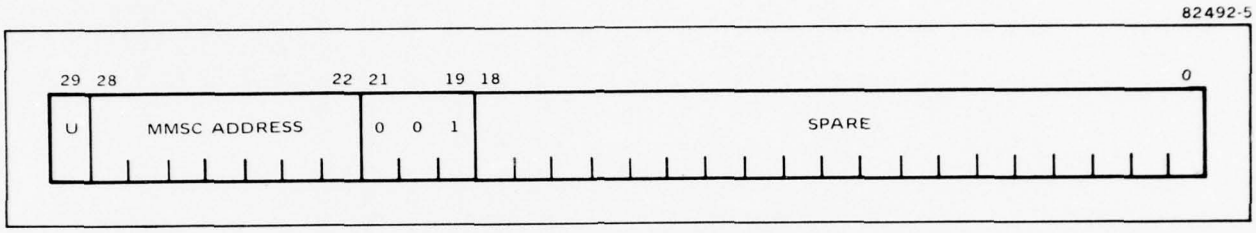
Code							Console
28	27	26	25	24	23	22	
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	1	0	0	3
0	0	0	1	0	0	0	4
0	0	1	0	0	0	0	5
0	1	0	0	0	0	0	6
1	0	0	0	0	0	0	7
1	1	1	1	1	1	1	1 through 7

Bit 29 – unused – may be 1 or 0

FORMATS FOR MMSC/PDMU MEMORY CONTROL COMMAND WORDS

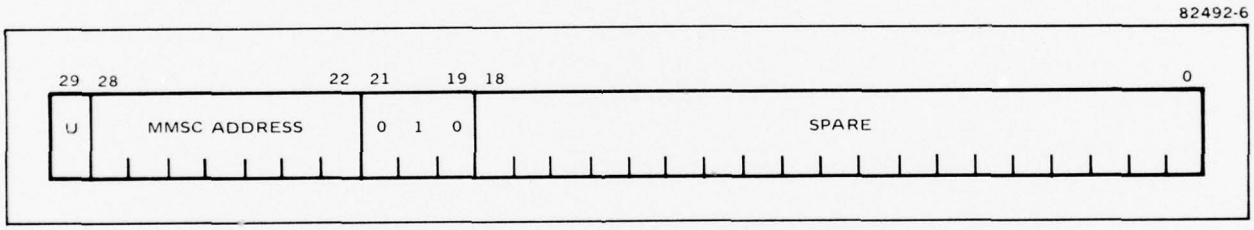
The MMSC/PDMU Memory Control Command Words consist of the memory load start, memory load stop, memory unload start, and memory unload stop.

Memory Load Start Description – The memory load start command causes the Memory Load FF to become set. With the Memory Load FF set, the MMSC or the PDMU will store output acknowledge words from the computer in its memory.



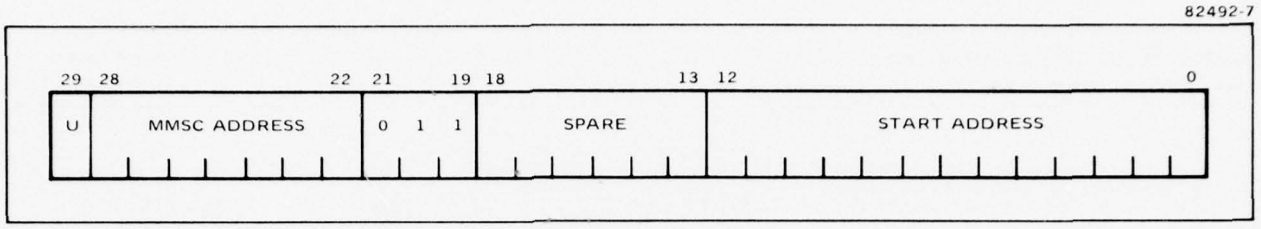
Format of Memory Load Start Word

Memory Load Stop Description – The memory load stop command causes the Memory Load FF to be reset. With the Memory Load FF reset, MMSC or PDMU will not store output acknowledge words in its memory.



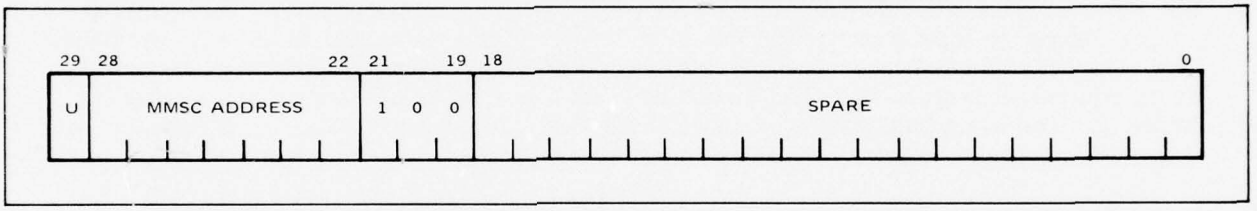
Format of Memory Load Stop Word

Memory Unload Start Description – The memory unload start command causes bits 0-12 to be loaded into the Output Data Address Counter and the Memory Unload FF to become set. With the Memory Unload FF set the MMSC or PDMU will access the memory address specified by the Output Data Address Counter, disassemble the 36 bit word into two 30 bit words, transmit the two words to the computer as input data request words and then increment the Output Data Address Counter. This process will continue until the Memory Unload FF is reset.



Format of Memory Unload Start Word

Memory Unload Stop Description – The memory unload stop command causes the Memory Unload FF to be reset. With the Memory Unload FF reset, the MMSC or PDMU will discontinue transmission of input data request words after the current transmission is complete.



Format of Memory Unload Stop Word

FORMATS FOR MMSC INDICATOR WORD AND PDMU PASSIVE FORMAT WORD

The MMSC Indicator Word and PDMU Passive Format word have the same word type. The Indicator Word is only used when addressing an MMSC while the Passive Format Word is used when addressing a PDMU.

Indicator Word (MMSC Only) – The format of MMSC Indicator words is shown in Figure A. There are 58 rear-projection readout devices in an MMSC each with 12 selectable lamps. Each lamp can display a different message in the readout. The lighting of the 58X12=696 lamps is under computer control via the indicator word. The coding for this information is given in Table I. Once a lamp is lit, it will remain lit until a new indicator word is sent to either blank the readout or change to a new lamp within the readout. The correlation of the readout coding to panel location of the readout is shown in Figure B.

In addition to the 12 selectable labels, the alert readouts have 3 selectable backgrounds. These are indicated as background 1, 2, and blank. When a particular background is selected, all four of the alert readouts will be illuminated or blanked by the selection. To activate the background requires sending an external function indicator word with the desired AL code. No lamp driver no., cell no., or lamp code must be specified as is required to light a particular label on an alert. It is intended that one of the background colors be used as an operational or tactical alert while the other will be used as an equipment fault alert. The codes for selecting the backgrounds are specified in Table II. The alert background must be in the blank state when either background 1 or 2 is initiated to prevent two colors being on simultaneously.

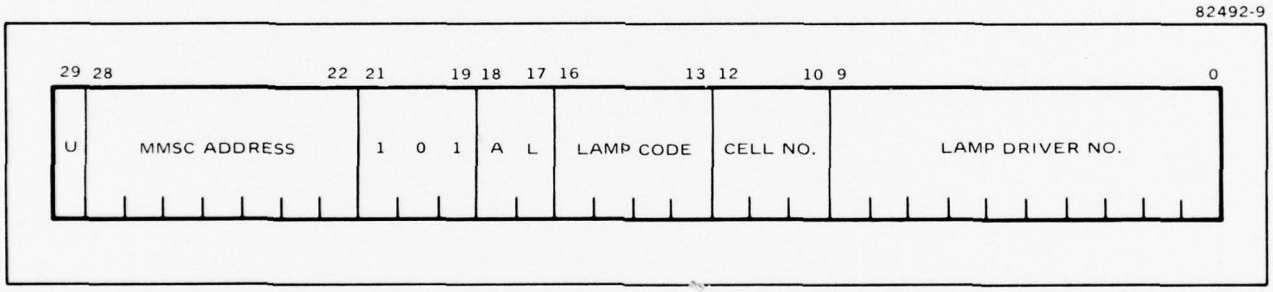


Figure A. Format of MMSC Indicator Words

TABLE I. INDICATOR WORD CODING

Bits 0 – 9 — Lamp Driver Code

9	8	7	6	5	4	3	2	1	0	Lamp Driver No.
0	0	0	0	0	0	0	0	0	0	None
0	0	0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	0	1	0	0	3
0	0	0	0	0	0	1	0	0	0	4
0	0	0	0	0	1	0	0	0	0	5
0	0	0	0	1	0	0	0	0	0	6
0	0	0	1	0	0	0	0	0	0	7
0	0	1	0	0	0	0	0	0	0	8
0	1	0	0	0	0	0	0	0	0	9
1	0	0	0	0	0	0	0	0	0	10
1	1	1	1	1	1	1	1	1	1	1 thru 10

Bits 10 – 12 — Cell Number Code

12	11	10	Octal		
0	0	0	0	None	
0	0	1	1	Cell	1
0	1	0	2		2
0	1	1	3		3
1	0	0	4		4
1	0	1	5		5
1	1	0	6		6
1	1	1	7	None	

Bits 13 – 16 — Lamp Number Code

16	15	14	13	Octal	Lamp Number
0	0	0	0	00	1
0	0	0	1	01	2
0	0	1	0	02	3
0	0	1	1	03	4
0	1	0	0	04	5
0	1	0	1	05	6
0	1	1	0	06	7
0	1	1	1	07	8
1	0	0	0	10	9
1	0	0	1	11	10
1	0	1	0	12	11
1	0	1	1	13	12
1	1	0	0	14	5 and 9
1	1	0	1	15	6 and 10
1	1	1	0	16	11
1	1	1	1	17	Blank

FORMATS FOR MMSC INDICATOR WORD (Continued)

TABLE II.

Bits 17 – 18	(AL) Alert Background Code		
18	17	Octal	
0	0	0	None
0	1	1	Background 1
1	0	2	Background 2
1	1	3	Blank Background

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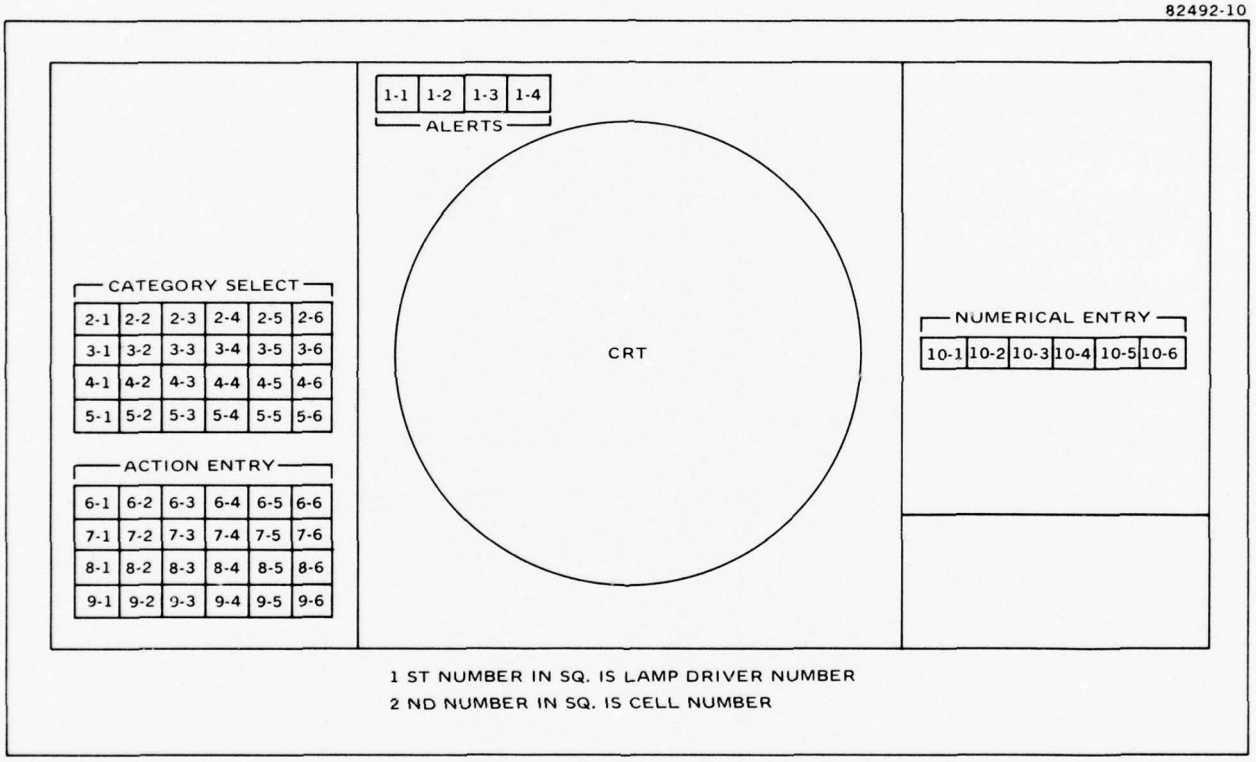


Figure B. MMSC Readout Coding

Passive Format Word (PDMU Only) – The passive format word contains the format code which is stored in a register. The format code specifies the number and placement of the data beams on the MMSC display.

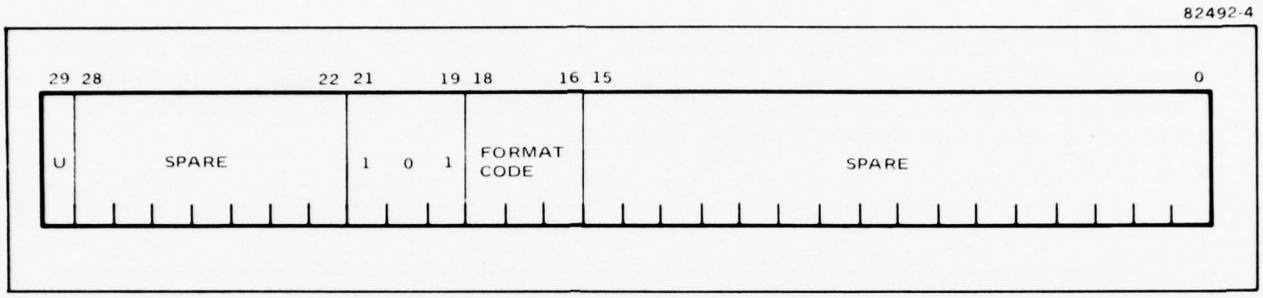


Figure C. Coding of the Passive-Format Word to Control MMSC Display of Data Beams

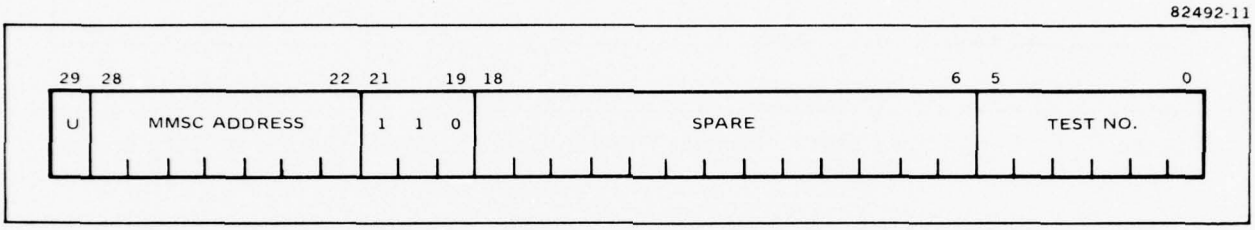
Format				Display Parameters*
18	17	16	Octal	
0	0	0	0	No Display – I/O Operations Only
0	0	1	1	680 Lines, 144 Beams Full Width
0	1	0	2	340 Lines, 288 Beams Full Width
0	1	1	3	680 Lines, 144 Beams Left Half
1	0	0	4	680 Lines, 72 Beams (1-72) Full Width
1	0	1	5	680 Lines, 72 Beams (73-144) Full Width
1	1	0	6	680 Lines, 72 Beams (1-72) Half Width
1	1	1	7	680 Lines, 72 Beams (73-144) Half Width

*Refer to Section 4 for detailed display information.

FORMAT FOR TEST STIMULUS WORD

The test stimulus word initiates an auto-test specified by the test number in bits 0-5.

The test stimulus word initiates an auto-test. The specific auto-test to be performed is specified by the test number in bits 0-5. The codes for the auto-tests are defined in the table. Use of the test stimulus words to perform auto-testing is described in Diagnostic Programming, Software Memo-Volume II.



Format of Test Stimulus Word

TEST STIMULUS WORD

Bits 0 – 5

Test Number

5	4	3	2	1	0	Octal	Test
0	0	0	0	0	0	00	Auto-Test Unit
0	0	0	0	0	1	01	I/O Unit
0	0	0	0	1	0	02	I/O Counters
0	0	0	0	1	1	03	Frame Rate Generator
0	0	0	1	0	0	04	Spare
0	0	0	1	0	1	05	Memory Data Register - 1
0	0	0	1	1	0	06	Memory Data Register - 2
0	0	0	1	1	1	07	Display Generator
0	0	1	0	0	0	10	Line Counter
0	0	1	0	0	1	11	G. P. Counters
0	0	1	0	1	0	12	Registers
0	0	1	0	1	1	13	Address Register 1
0	0	1	1	0	0	14	Address Register 2
0	0	1	1	0	1	15	Address Register 3
0	0	1	1	1	0	16	Address Register 4
0	0	1	1	1	1	17	Address Register 5
0	1	0	0	0	0	20	Symbol Address Register
0	1	0	0	0	1	21	Data Stop
0	1	0	0	1	0	22	Raster Generator
0	1	0	0	1	1	23	Time Compression
0	1	0	1	0	0	24	Intensity 1
0	1	0	1	0	1	25	Intensity 2
0	1	0	1	1	0	26	Intensity 3
0	1	0	1	1	1	27	Symbol Generator
0	1	1	0	0	0	30	Deflection 1
0	1	1	0	0	1	31	Deflection 2
0	1	1	0	1	0	32	Display Control
0	1	1	0	1	1	33	Display Control Counter
0	1	1	1	0	0	34	Program Control Counter
0	1	1	1	0	1	35	Spare
0	1	1	1	1	0	36	Spare
0	1	1	1	1	1	37	Spare
1	1	1	1	1	1	77	Auto-Test Unit

FORMAT FOR OUTPUT ACKNOWLEDGE WORDS

Two 30-bit output acknowledge words are used to form one 36-bit MMSC or PDMU memory word.

Output acknowledge words are sent from the computer and used to load the memory and to provide bit patterns for auto-testing. Output acknowledge words consist of two types, designated word 1 and word 2. Successive transmission of word 1 and a word 2 is required to form a 36-bit memory word. The 36-bits obtained from the 2 words are assembled in the Input Register. The Input Register data is then stored in the address specified by the Input Data Address Counter if the memory load FF is set.

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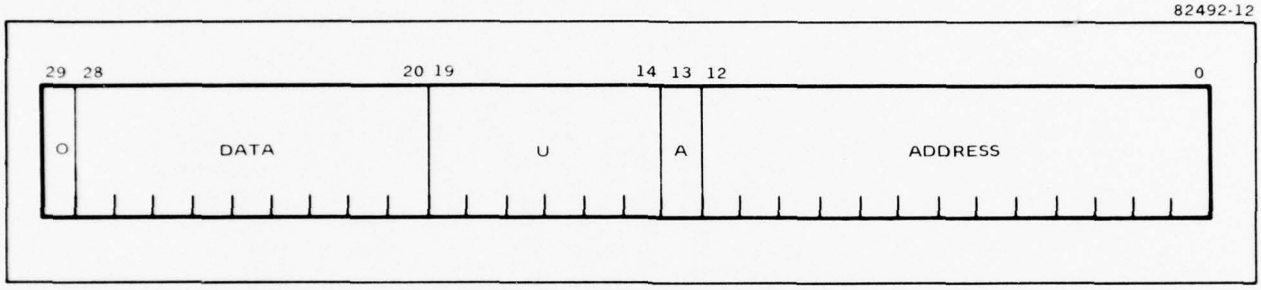
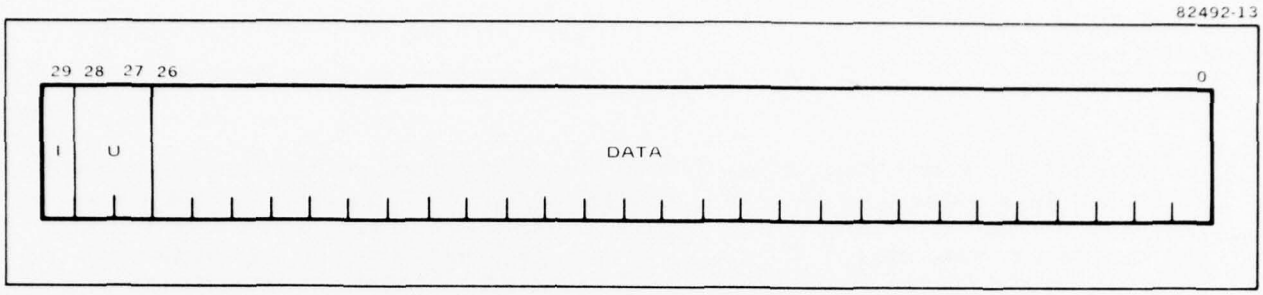


Word 1 of the Output Acknowledge Word Pair

Description	
Bits 0 – 12	Contains a 13 bit address which is loaded into bits 0-12 of the Input Data Address Counter when bit 13 is true.
Bit 13	A = 0, increment the Input Data Address Counter by 1. A = 1, load bits 0-12 into the Input Data Address Counter.
Bits 14 – 19	Unused
Bits 20 – 28	Contains data which is loaded into bits 27-35 of the Input Register.
Bit 29	Always a 0 to indicate word 1.

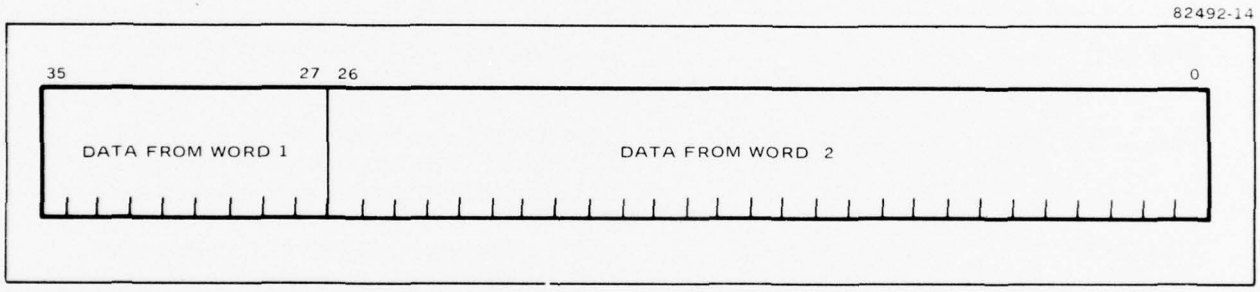


Word 2 of the Output Acknowledge Word Pair

Description

Bits 0 – 26	Contains data which is loaded into bits 0-26 of the Input Register.
Bits 27 – 28	Unused
Bit 29	Always a 1 to indicate word 2.

The reception of word 2 and memory load FF set is a command to store the word in the Input Register in the memory location specified by the Input Data Address Counter. The format of the resulting memory word is:



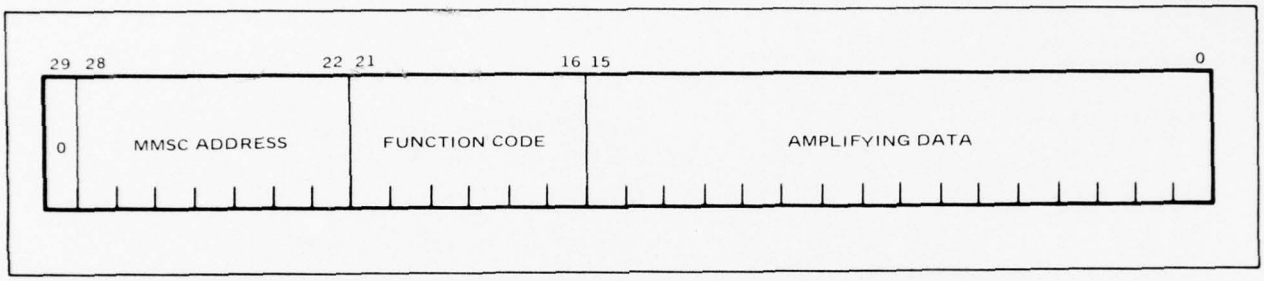
Format of Memory Word

COMPUTER NOTIFICATION OF MMSC ACTIONS: INTERRUPT WORD FORMAT

Interrupt words are sent to the computer from an MMSC to notify the computer of actions occurring at a console.

An interrupt will result when an action entry, numerical entry, number entry, keyboard or the initiate pushbutton is depressed. (See facing figure.) Only one interrupt will result from a single depression of a pushbutton. Interrupts will also result when rolling the trackball or when the end of a display frame is reached before all information has been displayed. During auto-testing, the interrupt is used to inform the computer of test results.

82492-65



General Interrupt Word Format

Word Format Description

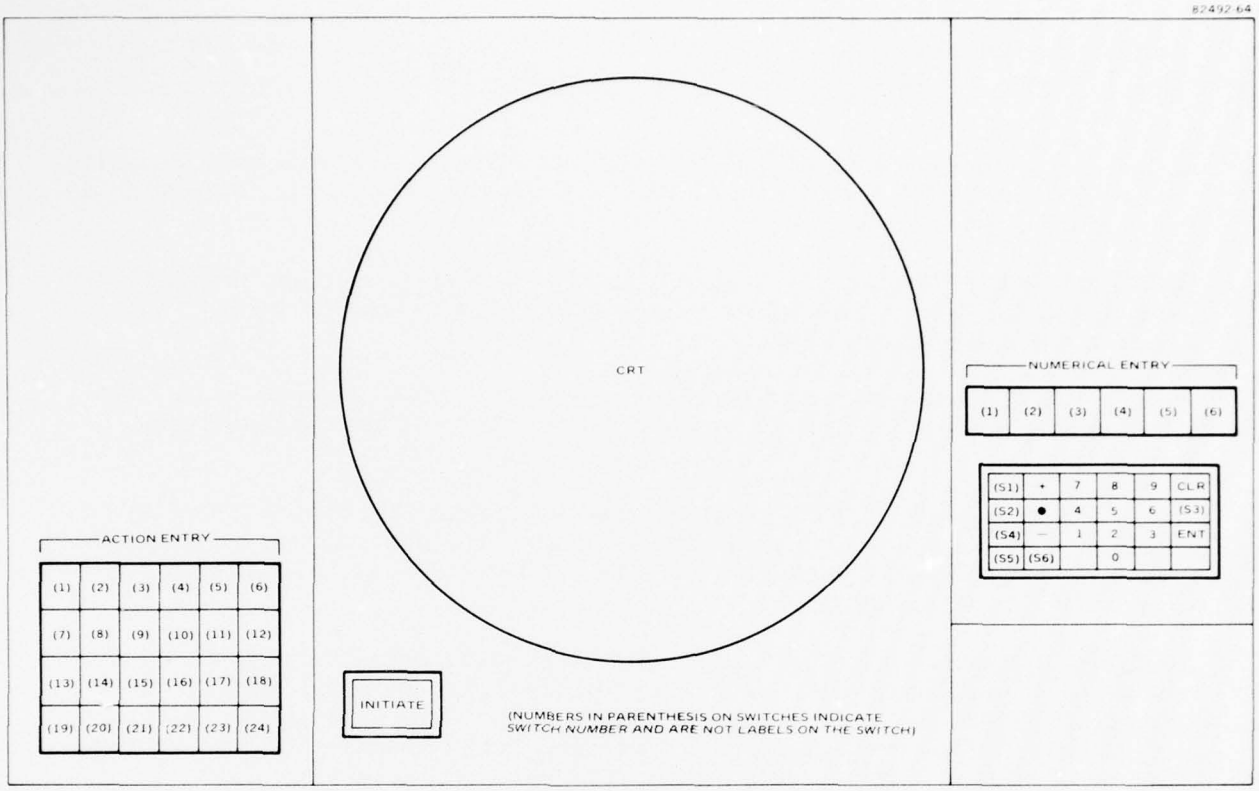
Bits 0-15 — Contains amplifying data used to supplement the function code

Bits 16-21 — Function code – defines the type of interrupt word. The codes for the functions are defined in the table of the next topic.

Bits 22-28 — MMSC address – defines to the computer the MMSC which transmitted the interrupt. Only one of the 7 bits will be set.

Code							Console
28	27	26	25	24	23	22	
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	1	0	0	3
0	0	0	1	0	0	0	4
0	0	1	0	0	0	0	5
0	1	0	0	0	0	0	6
1	0	0	0	0	0	0	7

Bit 29 — Always 0



MMSC Front Panel Pushbutton Locations

MMSC FUNCTION CODES

Function codes for the Action Entry, Numerical Entry, and Initiate switches, located on the front panel of the MMSC are presented in the table, together with those of the Display Overflow, Auto-Test Response functions, Number Entry, Trackball and Keyboard.

Action Entry – The function codes for the action entry switches are listed in the facing table. The correlation of switch number to panel location of the switch is shown in the figure of the previous topic.

Numerical Entry – The function codes for the numerical entry switches are listed in the facing table. The correlation of switch number to panel location of the switch is shown in the figure on page 1-15.

Initiate – The initiate pushbutton is located in the lower left-hand corner of the CRT panel (see figure in previous topic.) The function code for initiate is listed in the facing table.

Display Overflow – When MMSC reaches the end of its specified display frame before all data has been displayed, an interrupt will occur. The interrupt will be transmitted once each frame until the problem is corrected. The function code for display overflow is listed in the facing table.

Auto-Test Response – In response to an external function test stimulus word, an MMSC will transmit an interrupt word consisting of the function code listed in the facing table and amplifying data A-1 (next topic). The amplifying data A-1 varies with the type of test initiated. This data is specified in Diagnostic Programming, Software Memo-Volume II.

The Number Entry, Trackball, and Keyboard interrupt words all contain amplifying data. These words are presented in the next two topics.

FUNCTION CODES

Switch/Action Description		Interrupt Word Bits							Amplifying Code Type
		21	20	19	18	17	16	Octal	
Action Entry Switch	1	0	0	0	0	0	1	01	All Zero
	2	0	0	0	0	1	0	02	
	3	0	0	0	0	1	1	03	
	4	0	0	0	1	0	0	04	
	5	0	0	0	1	0	1	05	
	6	0	0	0	1	1	0	06	
	7	0	0	0	1	1	1	07	
	8	0	0	1	0	0	0	10	
	9	0	0	1	0	0	1	11	All Zero

FUNCTION CODES (Continued)

Switch/Action Description		Interrupt Word Bits							Amplifying Code Type
		21	20	19	18	17	16	Octal	
Action Entry Switch	10	0	0	1	0	1	0	12	All Zero
	11	0	0	1	0	1	1	13	
	12	0	0	1	1	0	0	14	
	13	0	0	1	1	0	1	15	
	14	0	0	1	1	1	0	16	
	15	0	0	1	1	1	1	17	
	16	0	1	0	0	0	0	20	
	17	0	1	0	0	0	1	21	
	18	0	1	0	0	1	0	22	
	19	0	1	0	0	1	1	23	
	20	0	1	0	1	0	0	24	
	21	0	1	0	1	0	1	25	
	22	0	1	0	1	1	0	26	
	23	0	1	0	1	1	1	27	
	24	0	1	1	0	0	0	30	
Numerical Entry Switch	1	0	1	1	0	0	1	31	
	2	0	1	1	0	1	0	32	
	3	0	1	1	0	1	1	33	
	4	0	1	1	1	0	0	34	
	5	0	1	1	1	0	1	35	
	6	0	1	1	1	1	0	36	
Initiate		0	1	1	1	1	1	37	
Display Overflow		1	0	0	0	0	0	40	All Zero
Auto-Test Response		1	0	0	0	0	1	41	A-1
Number Entry		1	0	1	0	0	0	50	A-2
Trackball		1	1	0	0	0	0	60	A-3
Keyboard		1	1	1	0	0	0	70	A-4

AMPLIFYING DATA FOR THE NUMBER ENTRY AND TRACKBALL INTERRUPT

A list of the amplifying data for the Number Entry Panel and Trackball are tabulated and described.

Number Entry Panel – The interrupt word for switches on the number entry panel consists of a fixed function code plus amplifying data A-2 which depends on the specific button pushed on the number entry panel. The function code is listed in the table of the previous topic. The amplifying data A-2 is specified in the facing table. The correlation of pushbutton symbol to panel location of the pushbutton is shown in the figure on page 1-15.

Trackball – Trackball increments are transmitted to the computer by interrupt once each frame if the increment counters are detected to be non-zero. The interrupt word consists of a fixed function code plus amplifying data A-3 which specifies the ΔX and ΔY increments. The ΔX and ΔY increments represent the circumferential distance in X and Y that the surface of the trackball has been displaced since the last frame. If the trackball is being rotated at a high speed such that the increment counters reach all ones, the counters will remain in the all ones state until the increments are sent to the computer. The counters are then reset to begin the next accumulation. This allows the display system to follow maximum ball rate movements of 23.1 in/sec when in the 35 frame per second mode and 33 in/sec when in the 50 frames per second mode. This corresponds to CRT movement of the trackball of 8.4 in/sec and 12 in/sec respectively in X and Y when maximum resolution is utilized. The function code for the trackball word is listed in the table of the previous topic. The format for the amplifying data is specified in the facing table.

AMPLIFYING DATA CODES

Code Description		Interrupt Word Bits																
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
A-1 (Auto-Test)		Bit patterns are given for each test in Diagnostic Programming, Software Memo Volume II																
A-2 (Number Entry)																		Octal
Spare Switch	S1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	41
	S2	|	|	|	|	|	|	|	|	|	|	1	0	0	0	1	0	42
	S3	|	|	|	|	|	|	|	|	|	|	1	0	0	0	1	1	43
	S4	|	|	|	|	|	|	|	|	|	|	1	0	0	1	0	0	44
	S5	|	|	|	|	|	|	|	|	|	|	1	0	0	1	0	1	45
	S6	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	46

AMPLIFYING DATA CODES (Continued)

Code Description	Interrupt Word Bits																
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Octal
Enter	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	50
Clear											1	0	1	0	0	1	51
Plus											1	0	1	0	1	1	53
Minus											1	0	1	1	0	1	55
Decimal Point											1	0	1	1	1	0	56
0											1	1	0	0	0	0	60
1											1	1	0	0	0	1	61
2											1	1	0	0	1	0	62
3											1	1	0	0	1	1	63
4											1	1	0	1	0	0	64
5											1	1	0	1	0	1	65
6											1	1	0	1	1	0	66
7											1	1	0	1	1	1	67
8											1	1	1	0	0	0	70
9							0	0	0	0	1	1	1	0	0	1	71
A-3 (Trackball)	0	0	0	0	0	0	S y	M y3	M y2	M y1	M y0	S x	M x3	M x2	M x1	M x0	

S = Sign: "0" = + Direction
"1" = - Direction

M = Magnitude

M_0 = 1 = 0.044 in. *
M_1 = 1 = 0.088 in.
M_2 = 1 = 0.176 in.
M_3 = 1 = 0.352 in.

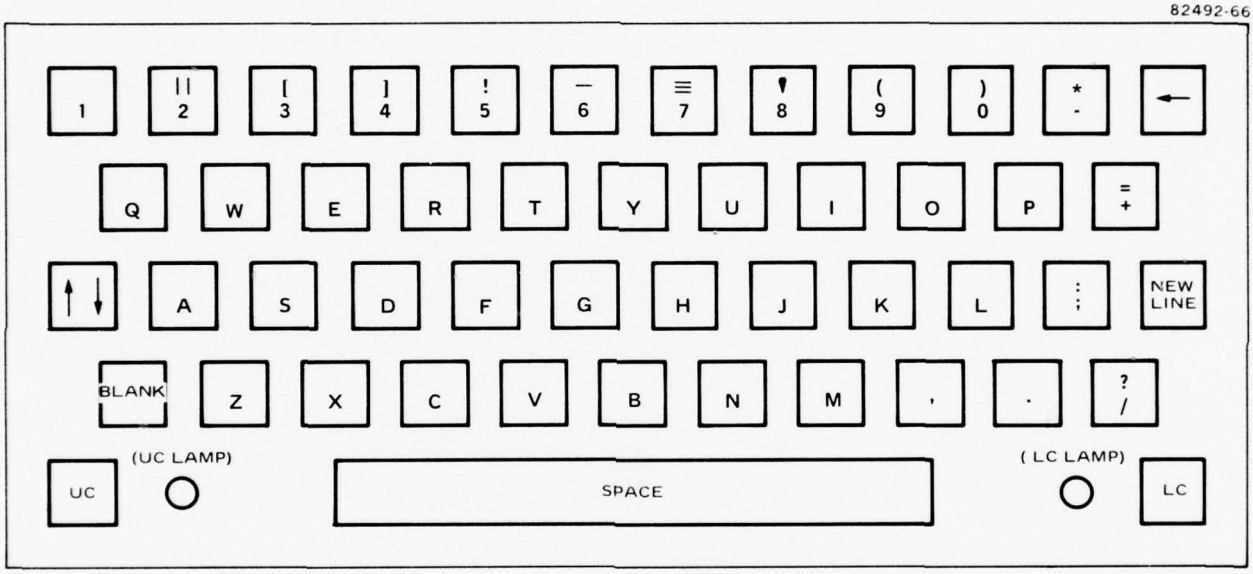
*Inches of ball surface movement.

AMPLIFYING DATA FOR THE KEYBOARD INTERRUPT WORD

The amplifying data for the interrupt word of switches on the keyboard panel, located on the bullnose of the MMSC console, are listed and described.

The interrupt word for switches on the keyboard panel consists of a fixed function code plus amplifying data A-4 (see facing table) which depends on the specific button pushed on the keyboard. The function code is listed in the table on 1-16. The correlation of pushbutton symbol to pushbutton location on the keyboard is shown in the figure below. It should be noted that the upper/lower case selection is controlled by the two switches on the keyboard labeled UC and LC. The lamp adjacent to each switch determines which switch is activated. Activating one switch automatically resets the other.

82492-66



Console Keyboard Panel

AMPLIFYING DATA CODES (Continued)

Code Description	Interrupt Word Bits																
A-4 (Keyboard)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Octal
↓ (Down 1 line) (LC)	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	012
New Line											0	0	1	1	0	1	015
Space											1	0	0	0	0	0	040
+ (Plus)											1	0	1	0	1	1	053
, (Comma)											1	0	1	1	1	1	054
- (Minus)											1	0	1	1	0	1	055
. (Period - Dec. Point)		·									1	0	1	1	1	0	056
/ (Slash)											1	0	1	1	1	1	057
ø											1	1	0	0	0	0	060
1											1	1	0	0	0	1	061
2											1	1	0	0	1	0	062
3											1	1	0	0	1	1	063
4											1	1	0	1	0	0	064
5											1	1	0	1	0	1	065
6											1	1	0	1	1	0	066
7											1	1	0	1	1	1	067
8											1	1	1	0	0	0	070
9											1	1	1	0	0	1	071
; (Semi-colon)											1	1	1	0	1	1	073
Blank										0	1	1	1	1	1	1	077
A										1	0	0	0	0	0	1	101
B										1	0	0	0	0	1	0	102
C										1	0	0	0	0	1	1	103
D										1	0	0	0	1	0	0	104
E										1	0	0	0	1	0	1	105
F										1	0	0	0	1	1	0	106
G										1	0	0	0	1	1	1	107
H										1	0	0	1	0	0	0	110
I										1	0	0	1	0	0	1	111
J										1	0	0	1	0	1	0	112
K	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	113

AMPLIFYING DATA FOR THE KEYBOARD INTERRUPT WORD (Continued)

AMPLIFYING DATA CODES (Continued)

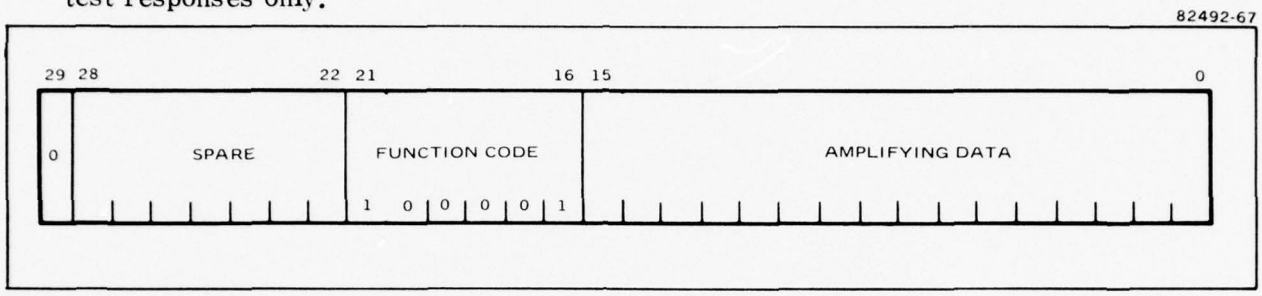
Code Description	Interrupt Word Bits																
A-4 (Continued)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Octal
L	0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	0	114
M										1	0	0	1	1	0	1	115
N										1	0	0	1	1	1	0	116
O										1	0	0	1	1	1	1	117
P										1	0	1	0	0	0	0	120
Q										1	0	1	0	0	0	1	121
R										1	0	1	0	0	1	0	122
S										1	0	1	0	0	1	1	123
T										1	0	1	0	1	0	0	124
U										1	0	1	0	1	0	1	125
V										1	0	1	0	1	1	0	126
W										1	0	1	0	1	1	1	127
X										1	0	1	1	0	0	0	130
Y										1	0	1	1	0	0	1	131
Z										1	0	1	1	0	1	0	132
← (Back Space)									0	1	0	1	1	1	1	1	137
↑ (Up 1 Line (UC)									1	0	0	0	1	0	1	0	212
= (Equal)									1	0	1	0	1	0	1	1	253
* (Asterisk)									1	0	1	0	1	1	0	1	255
? (Question Mark)									1	0	1	0	1	1	1	1	257
) (Right Paren)									1	0	1	1	0	0	0	0	260
" (Quotation Mark)									1	0	1	1	0	0	1	0	262
[(Left Bracket)									1	0	1	1	0	0	1	1	263
] (Right Bracket)									1	0	1	1	0	1	0	0	264
! (Exclamation)									1	0	1	1	0	1	0	1	265
_ (Underline)									1	0	1	1	0	1	1	0	266
≡ (Equivalence)									1	0	1	1	0	1	1	1	267
' (Apostrophe)									1	0	1	1	1	0	0	0	270
((Left Paren)									1	0	1	1	1	0	0	1	271
: (Colon)	0	0	0	0	0	0	0	0	1	0	1	1	1	0	1	1	272

1-22/1-23 BLANK PAGE FOLLOWS

COMPUTER NOTIFICATION OF PDMU ACTIONS: INTERRUPT WORDS

The interrupt word for Auto-Test Response, which is the only one that is sent to the computer from a PDMU, is formatted and described.

Auto-Test Response – Interrupt words are sent to the computer from a PDMU with auto-test responses only.



Interrupt Word Format

Description	
Bits 0 – 15	Contains auto-test responses
Bits 16 – 21	Function code is always the auto-test code 41
Bits 22 – 28	Spare
Bit 29	Always a 0.

USE OF MMSC IN COMPUTER TO PDMU COMMUNICATIONS

The MMSC operator specifies passive display format parameters via the computer.

There is no electrical connection for direct MMSC to PDMU communication. The system computer must contain as part of its program, routines to convert console action entry, numerical entry and/or keyboard interrupts into PDMU format external function words. Since the computer controls PDMU operations, other input devices connected to it such as typewriters, keysets, etc. could also be utilized to specify passive display formats. When a PDMU drives several consoles, all with passive display selected, will observe the same passive display data and in the same format.

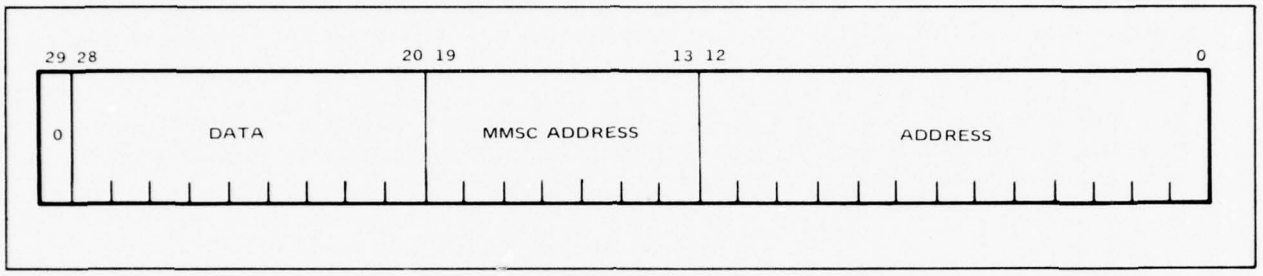
The PDMU contains no operator panels, only a maintenance panel and a power panel. By placing the PDMU off-line from the computer the maintenance panel may be used to simulate any computer word or message.

DATA WORDS TO COMPUTER FROM MMSC OR PDMU: INPUT DATA REQUEST WORDS

Input data request words are sent to the computer from an MMSC or a PDMU during a memory unload process and during certain auto-tests.

A memory word consisting of 36 bits is loaded into the Output Register and then disassembled into two 30 bit words to be transmitted to the computer as word types 1 and 2. Input data request words result only from either a memory unload command or certain auto-test commands from the computer.

82492-68



Word 1 Format

Bits 0 – 12

Data address – contains the contents of the Output Data Address Counter. During memory unload this address is the memory address from which the current data word being transmitted was extracted.

Bits 13 – 19

These bits are all zeros for the PDMU. In the MMSC, they contain the address of the MMSC transmitting the input data request word.

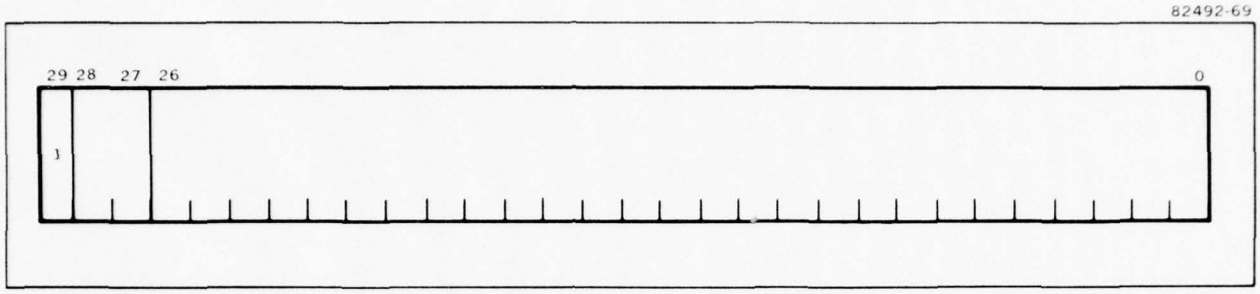
Code							Console
19	18	17	16	15	14	13	
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	1	0	0	3
0	0	0	1	0	0	0	4
0	0	1	0	0	0	0	5
0	1	0	0	0	0	0	6
1	0	0	0	0	0	0	7

Bits 20 – 28

Contains the data stored in bits 27-35 of the memory word being transmitted.

Bit 29

Always a 0 to indicate word 1.



Word 2 Format

Bits 0 – 26	Contains the data stored in bits 0-26 of the memory word being transmitted.
Bits 27 – 28	May be "0"s or "1"s should be ignored.
Bit 29	Always a 1 to indicate word 2. Input data request words are always transmitted in pairs with word 2 always transmitted following word 1. In the case of the MMSC, word 2 will always be transmitted from the same MMSC as the previously transmitted word 1. This eliminates any ambiguities when more than two consoles are commanded to unload their memories.

SECTION 2
MEMORY ALLOCATIONS

MMSC AND PDMU MEMORY ALLOCATIONS

The MMSC memory is partitioned into three storage blocks and the PDMU memory is partitioned into two storage blocks, with allocations as defined below.

MMSC Memory Allocations – The MMSC memory (see Table I) is partitioned into three blocks for storage of the various types of MMSC memory words. The MMSC instruction words, are stored in octal locations 00000 through 00377. Symbol code words and line words (for lines-type II) are stored in the last 1024 locations 16000 through 17777. Position, line and alphanumeric words may be stored at any location in memory not in use for an instruction word or a symbol code word. Normally, these words will be stored between the instruction word store and the symbol code store, i.e., 00400 through 15777.

PDMU Memory Allocations – The PDMU memory (see Table II) is partitioned into two sections: instruction word store and intensity word store. The first 32 locations, octal 00000 through 00037, are for storage of instruction words only. The remainder of the PDMU memory is for storage of passive sonar display intensity words.

If the MMSC or PDMU memory is being used as a bulk storage device, there are no restrictions as to the placement of data. In this case, all memory locations are available for storage of data.

TABLE I. MMSC MEMORY MAP

00000 ↓ 00377	instruction words
00400 ↓ 15777	position, line, and alphanumeric words
16000 ↓ 17777	symbol code words

TABLE II. PDMU MEMORY MAP

00000 ↓ 00037	instruction words
00040 ↓ 17777	passive display intensity words

8 2 4 9 2

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SECTION 3
MMSC PROGRAMMING

GENERAL DESCRIPTION OF THE MULTI-MODE SONAR CONSOLE DISPLAY PROGRAM

The Multi-Mode Sonar Console controls the storing, selecting, processing and displaying of non-passive data.

General Description – The display of non-passive data on the CRT of a Multi-Mode Sonar Console is directly controlled by the contents of its memory. The information within its memory is divided into two basic sections; a program and a data bank. The program controls general display parameters such as frame rate, the form of presentation, and describes the type of data contained within a block of words in the data bank. In addition, the program controls the cycling through the data section of memory. This can be performed in a random manner under program control to optimize system operation. The data section of memory contains the detailed information for display such as the coordinate position for a sonar symbol and the data required to paint a symbol at that point.

Display Modes – The display of memory data is accomplished by using one or more display modes. The terminology "display mode" refers to a sequence of hardware logic operations that result in display of an individual symbol, alphanumeric or line. See table on opposite page. This is not to be confused with operational modes such as active search, track, etc.

Single Symbol Mode – The Single Symbol Mode is the basic console operating mode. In this mode of operation a position word is read from memory and the CRT beam is positioned to the coordinates specified therein. The symbol generator is loaded with one or more symbol code words which define a symbol shape from memory. The symbol is then displayed. When the display is complete, another position word is read and the cycle repeated. The term "symbol" in this document refers to anything displayed that uses the symbol generator. Operationally this may be sonar events, track symbols, alphanumerics, etc.

Track symbols, ball tab, hook markers and similar symbols are designated as processed data symbols and are displayed in the single symbol mode.

Line Type I Mode – The Line Type I Mode displays a line using a position word and a line word which are read from consecutive memory locations. The symbol address in the position word is not used.

Line Type II Mode – The Line Type II Mode is similar to Line Type I except the line word is stored in the symbol code store area of memory and the symbol address in the position word is used to retrieve the line word. This mode was included to simplify display of sonar events that are short lines.

In-Line Alphanumeric Mode – The In-Line Alphanumeric Mode is used to display a horizontal line of A-N characters. A position word is used to define the coordinates of the first character. The symbol address in the position word is not used. Alphanumerics words follow the position word with each defining four characters. After display of a character the CRT beam is automatically positioned a small increment to the right. Additional position words are used for vertical spacing of character lines. This mode of operation does not save display time over the single symbol mode. It does however, conserve memory locations.

NON-PASSIVE DISPLAY MODES

Mode	Display Form
Single Symbol	To Protray Sonar Events, Tracks, Alphanumerics, Ball Tab, Hook Marker, etc.
Line Type I	Long Lines Up To 2 Inches
Line Type II	For Sonar Events That Are Short Lines
In-Line Alphanumeric	Horizontal Line of Alphanumeric Characters

MEMORY ADDRESSING BY MULTIPLEXING THE MEMORY ADDRESS REGISTER

The Program Counter, Display Address Counter, Symbol Address Counter and the input/output counters are multiplexed into the Memory Address Register for memory control.

There are five basic types of memory operation: 1) entry of new data from the computer, 2) retrieval of memory data for transmission to the computer, 3) retrieval of instruction words, 4) retrieval of display data words, and 5) memory testing. There are five counters that generate the memory addresses. These counters are multiplexed into the Memory Address Register. The memory loading/unloading operations with the computer were covered in Section 1. The remaining functions are described below.

Program Counter – The Program Counter is used to address MMSC display instruction words. (See the figure on the opposite page). The counter is set to zero at the start of each display frame and is incremented under control of the Program Control Sequence Counter. Whenever a format control word is read out, memory bits 0-7 are loaded into the Program Counter effecting an unconditional transfer. The Program Counter has 8 bits, it drives the 8 LSB's of the Memory Address Register. The 5 MSB's of the Memory Address Register are always a "0" when the register contains the program count, thus the Program Counter only accesses the first 256 memory locations.

Display Address Counter – The Display Address Counter is used to read out position, line and alphanumeric words. It is a 13 bit counter and may access all of the MMSC memory. However, it normally reads the words between the instruction word store and the start of the symbol code word storage. The Display Address Counter is preset by bits 0-12 of a data start instruction word.

Symbol Address Counter – The Symbol Address Counter generates the memory address for the readout of symbol code words. The counter is preset by data start, alphanumeric, and position words as indicated in the table. Bits 10, 11, 12, of the Memory Address Register are always a "1" when the register contains a symbol address. Bit 0 (LSB) of the counter is always forced to the "0" state when the counter is preset with a symbol address. Only the 8 LSB's may be incremented under control of the Display Control Counter. Bits 8, 9 (MSB's) store bits 22 and 23 of the data start word. The six bits of symbol address contained in the position word are loaded into the Symbol Address Counter in two ways as indicated in the table.

The 1024 words of symbol code storage are partitioned into 8 groups of 128 words each. The groups are specified by data start instruction words. Within each group the six bits from the position word or alphanumeric word specifies 64 symbol start addresses. When processed data symbols are used, two groups are combined to form a single group of 256 words with 64 start addresses.

In-Line Alphanumeric Address Register – The In-Line Alphanumeric Address Register is a shift register that stores the alphanumeric word. The register shifts after display of each A-N to provide the Symbol Address Counter with the 6 LSB's of start address.

82492-27

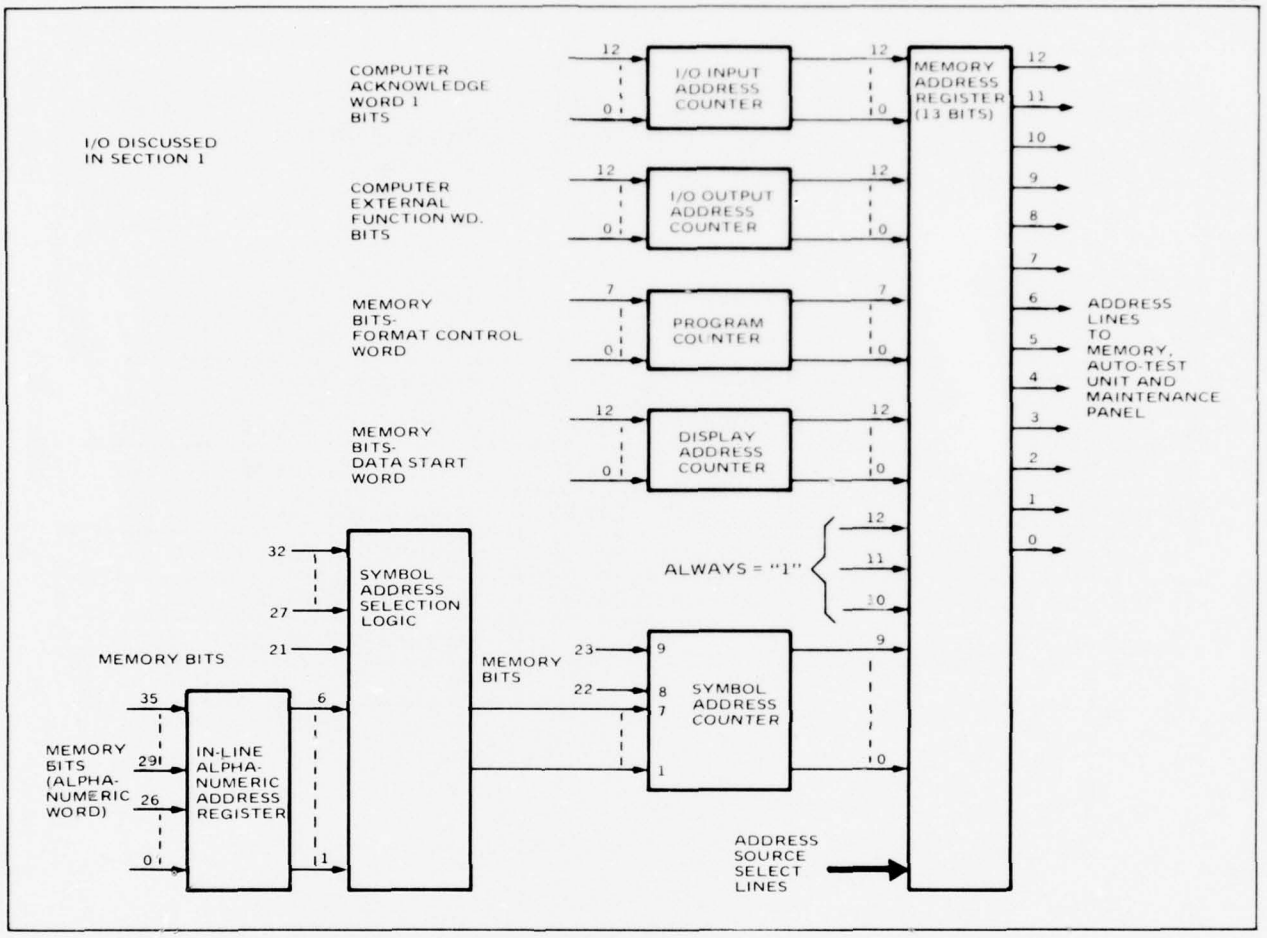


Diagram of the MMSC Memory Address

MEMORY ADDRESSING BY MULTIPLEXING THE MEMORY ADDRESS REGISTER (Continued)

SYMBOL ADDRESS COUNTER LOADING

In-Line Alphanumeric Mode	Single symbol mode for processed data symbol	Line type II mode and single symbol mode for other than processed data symbols	Symbol Address Counter
Data Start Bit 23	Data Start Bit 23	Data Start Bit 23	9
Data Start Bit 22	Data Start Bit 22	Data Start Bit 22	8
Data Start Bit 21	Position WD Bit 32	Data Start Bit 21	7
AN WD Bits 35, 20, 13, 6	Position WD Bit 31	Position WD Bit 32	6
AN WD Bits 34, 19, 12, 5	Position WD Bit 30	Position WD Bit 31	5
AN WD Bits 33, 18, 11, 4	Position WD Bit 29	Position WD Bit 30	4
AN WD Bits 32, 17, 10, 3	Position WD Bit 28	Position WD Bit 29	3
AN WD Bits 31, 16, 9, 2	Position WD Bit 27	Position WD Bit 28	2
AN WD Bits 30, 15, 8, 1	"0"	Position WD Bit 27	1
"0"	"0"	"0"	0

3-4/3-5 BLANK PAGE FOLLOWS

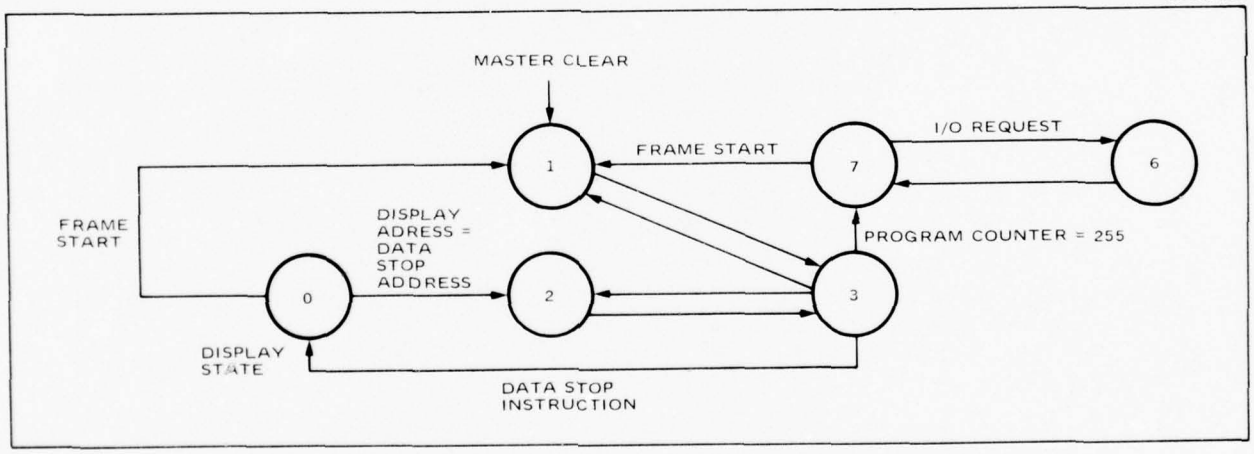
STATE DIAGRAMS FOR THE PROGRAM CONTROL COUNTER

Instruction words are retrieved from the memory by timing signals generated by the Program Control Counter.

The Program Control Counter is a sequence counter that generates the timing signals for the retrieval of instruction words. A state diagram of the counter is shown below. The various counter states are briefly explained in the table. Counter states 1, 2, 3 and 6 are 2 μsec in duration, states 0, and 7 are of variable length.

Characteristics of the counter of interest to one programming the MMSC are: Non-Valid instructions are any words in the first 256 MMSC memory locations with any of the following configurations for bits 33-35, 000, 010, 110, or 111. If there are a number of non-valid instruction words in consecutive locations the Program Control Counter sequences between states 2 and 3. Thus 4 μsec are used per non-valid instruction while the Program Control Counter is searching for a valid instruction. I/O unit requests for memory input or output are locked out. I/O requests are serviced in state 0 under control of the Display Control Counter. As indicated on the state diagram, a data stop instruction terminates the readout of instruction words by sequencing the Program Control Counter to state "0". The logic assumes a data stop instruction preceded by the data start instruction. It does not check that data start and data stop instructions are read out as a pair.

82492-28



State Diagram of the Program Control Sequence Counter

TABLE. PROGRAM CONTROL COUNTER

State	Action	Exit	Exit Conditions
1 (001)	Reset Memory Data Register to all "0"s. Transfer 8 LSB's of Memory Data Reg. (MDR) to Program Counter. Initiate memory read cycle.	1→3	Automatic
3 (011)	Load MDR with memory word.	3→0 3→1	Data stop word Frame start
	Determine from BITS 33-35 if word is a valid instruction.	3→2	Always except for frame start, data stop word, or Program Counter = 255
	If instruction, generate appropriate register load signal. Determine if Program Counter = 255	3→7	Program Counter = 255
2 (010)	Increment program counter unless word in MDR is a format control word. Initiate memory read cycle.	2→3	Automatic
0 (000)	Display the data defined by the data start and data stop instructions.	0→1	Frame start
		0→2	Always except if frame start occurs.
	Transfer memory control to the Display Control Counter.		
7 (111)	Rest state after display of all data prior to end of frame.	7→1 7→6	Frame start I/O input or output request.
6 (110)	Generate a memory read or write cycle for I/O unit if I/O request present.	6→7	Automatic

STATE DIAGRAMS FOR THE DISPLAY CONTROL COUNTER

The control of memory operations and display of memory data is accomplished by the Display Control Counter when a display mode is initiated.

The Display Control Counter is a 3 bit sequence counter which controls memory operations and display of memory data after a data stop instruction is read and processed.

State diagrams for each of the display modes are given in Figures A, B, and C. States 1, 2, 4, 5, 6, and 7 of the Display Control Counter have a duration of 2 μsec. The duration of state 3 is variable for symbols and alphanumerics in increments of 2 μsec.

When the Display Address Counter reaches the data stop address and the last symbol or line is displayed, control of the MMSC memory is transferred to the Program Control Counter.

DISPLAY CONTROL COUNTER SINGLE SYMBOL DISPLAY

State	Action	Exit	Exit Conditions
0	Rest state for display logic. Instruction words being processed.	0→1	Data stop word read out.
1	Transfer display address to Memory Address Register. Initiate memory read cycle.	1→2	Automatic
2	Finish display of last symbol.	2→0	End of display instr. (Data stop address or frame start).
	Increment Display Address Counter.	2→1	Word other than position word read out of memory.
	Load position word data into appropriate registers. Start CRT beam to symbol X, Y coordinates. Start settle time counter. Transfer symbol address to Memory Address Register. Initiate memory read.	2→3	Normal exit
3	Increment Symbol Address Counter. Load symbol generator with symbol code word. Repeat state 3 operations above until symbol code word bit 35 = 1. Service I/O unit memory requests.	3→1	Automatic when bit 35 of symbol code word = 1.

DISPLAY CONTROL COUNTER LINE DISPLAY

State	Action	Exit	Exit Conditions
0	Rest state for display logic. Instruction words being processed.	0→1	Date stop word read out.
1	Transfer display address to Memory Address Register. Initiate memory read cycle.	1→2	Automatic
2	Finish display of last line.	2→0	End of display instruct. or frame start.
	Increment Display Address Counter.	2→1	Wrong word order.
	Load position word data into appropriate registers. Start CRT beam to line start X, Y coordinates. Transfer display address to Memory Address Register for line type I or transfer symbol address for line type II. Initiate memory read.	2→3	Normal
3	Load symbol generator with line word. Service I/O memory input request.	3→4	Automatic
4	Service I/O memory output request. Start line display.	4→1	Automatic

82492-29

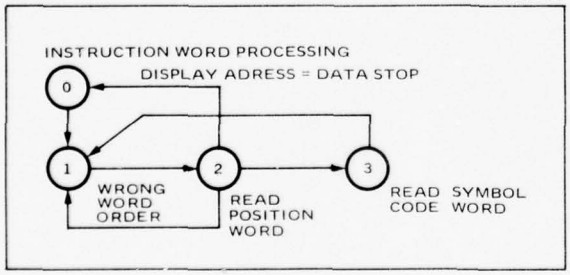


Figure A. State Diagram for Single Symbol Mode Display

82492-30

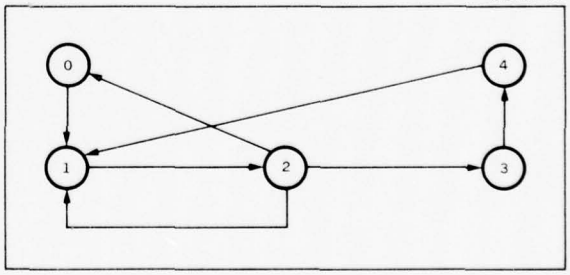


Figure B. State Diagram for Line Type I and II Display

STATE DIAGRAMS FOR THE DISPLAY CONTROL COUNTER (Continued)

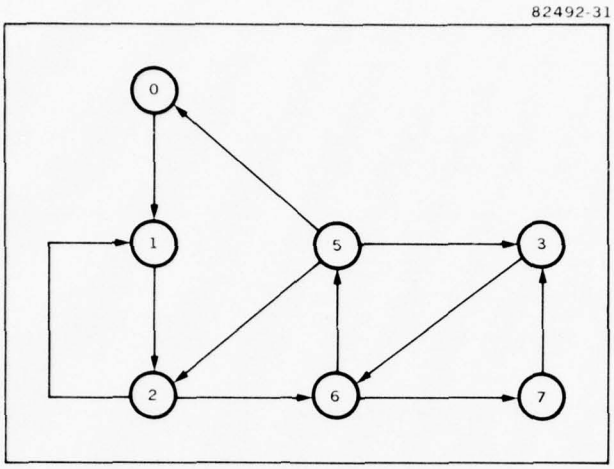


Figure C. State Diagram for In-Line Alphanumeric Display

DISPLAY CONTROL COUNTER IN-LINE ALPHANUMERICS

State	Operations	Exit	Exit Conditions
0	Rest state for display logic.	0 → 1	Data stop word read out.
1	Transfer display address to Memory Address Register. Initiate memory read cycle.	1 → 2	Automatic
2	Finish display of last alphanumeric.	2 → 1	Wrong word order. (Alphanumeric word read out).
	Increment Display Address Counter. Load position word data into appropriate registers.	2 → 6	Position word read out of memory.
	Start CRT beam to position of first alpha. Start settle time counter.		
6	If state 2 was prior state; transfer Display Address Counter to Memory Address Register. Initiate memory read.	6 → 5	If first alpha has not been displayed.
	If state 3 was prior state; service I/O unit output request. Shift Alphanumeric Address Register.	6 → 7	During display of 1st, 2nd, and 3rd alphanumeric.
7	Transfer symbol address to Memory Address Register. Initiate memory read cycle.	7 → 3	Automatic
3	Increment Symbol Address Counter. Load symbol generator with symbol code word. Repeat state 3 operations above until symbol code word bit 35 = 1. Service I/O unit input request.	3 → 6	Automatic after symbol code word bit 35 = 1
5	Increment Display Address Counter.	5 → 0	End of display, data stop address reached, or frame start.
	Load Alphanumeric Address Register with AN word. Shift first A-N address into Symbol Address Counter.	5 → 2	Position word read out.
	Transfer symbol address to Memory Address Register. Initiate memory read cycle.	5 → 3	Alphanumeric word read out.

DISPLAY PARAMETERS SPECIFIED BY FORMAT CONTROL WORD

The format control word specifies the basic display parameters, that apply to all display data.

There are four types of instructions used in an MMSC program. The Format Control Word. is discussed in this topic. The Time Compression Brightness Group Word, the Data Start Word, and the Data Stop Word are discussed in the following topic.

Format Control Word – The format control (see figure on opposite page) word specifies many of the display parameters that apply to all data displayed each frame. The format control word may also be used as a transfer instruction. See table on opposite page.

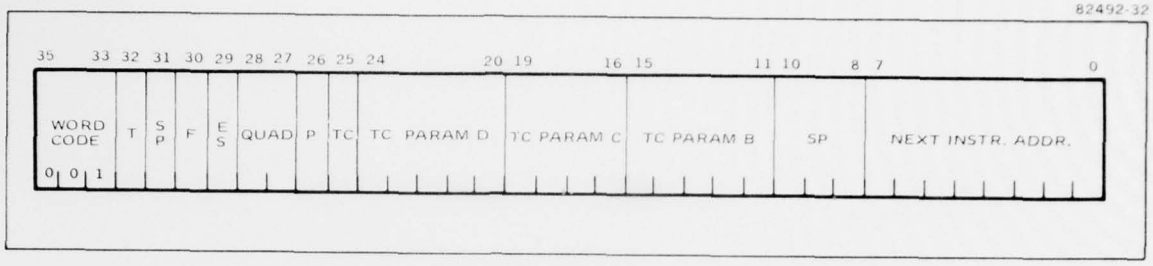
One format control word in memory is required to define certain display operations. The display control bits 11 through 31, are stored in a register which contains the data of the last format control word read out. Thus, placement of the word in the memory is not critical. The register is not reset at the end of a display frame.

The format control word may be used as a transfer since the Program Counter is forced to the address contained in bits 0-7. Display of data in a frame may be terminated by coding 377 in the next instruction field.

Format control words that transfer the program count to a lower numbered instruction address may create undesirable display effects. If a closed loop exists for the program counter that does not include address 377 (last program count) the data within the loop will be displayed at a rate higher than the frame rate which may cause degradation of the CRT phosphor.

Time Shared Formats – The MMSC memory can store more display data than can be processed in a display frame. This feature may be utilized to reduce computer-to-console data rates.

The MMSC memory may be loaded with two or more blocks of display data representing different operational formats or diagnostic test patterns. The computer would keep all formats updated as sensor data is processed. Changing a format would require transmission of only one or two format control instruction words to be used as transfer instructions.



Format Control Word

CODING OF CONTROL WORD

Bits 0-7 – Next instruction address.

Binary code, bit 0-LSB
bit 7-MSB

The Program Counter is always loaded with bits 0-7.

Bit 8-10 – Spare

Bit 11-15 – Time compression display interval in increments of the ping progression period.

Binary code, bit 11-LSB
bit 15-MSB

There is no zero display interval –
code 00000 = oldest ping only displayed
00001 = two oldest pings displayed
etc.

Bits 16-19 – Time compression ping progression period.

Binary code, bit 16-LSB
bit 19-MSB

Code 0000 = 1 frame
0001 = 2 frames, etc.

Bit 20-24 – Time compression dwell interval in increments of the frame period.

Binary code, bit 20-LSB
bit 24-MSB

Code 0000 = 1 frame
0001 = 2 frames, etc.

DISPLAY PARAMETERS SPECIFIED BY FORMAT CONTROL WORD (Continued)

CODING OF CONTROL WORD (Continued)

Bit 25 – Time compression BIT

TC = 0, The sonar events are displayed normally

TC = 1, The sonar events are displayed in a time compressed sequence. Display data not identified as sonar events will not be time compressed.

Refer to time compressed ping history topic for discussion of time compressed displays.

Bit 26 – Passive display bit

P = 0 Do not display input data from PDMU

P = 1 Display data from PDMU

When passive (PDMU) data is displayed the display of symbolic data stored in the MMSC memory is restricted to the time available in each frame following the display of all the passive data.

Bits 27-28 – Expanded sector quadrant designator.

28	27	
0	0	sector 180^{o}-270^{o}
0	1	sector 270^{o}-360^{o}
1	0	sector 90^{o}-180^{o}
1	1	sector 0^{o}- 90^{o}

Expanded sector data is displayed in the specified quadrant. Non-expanded sector data in the quadrant is blanked.

Refer to page 3-36
for discussion of expanded sector displays.

Bit 29 – Expanded sector bit

When set, the MMSC displays any block of data designated as expanded sector data in the ES quadrant. The data start instruction identifies the expanded sector data.

CODING OF CONTROL WORD (Continued)

Bit 30 – Frame rate bit

The display refresh rate is set from the computer with this bit for non-passive displays.

F = 0 = 35 frames/second
F = 1 = 50 frames/second

At the lower frame rate more symbols can be displayed. The higher rate allows a brighter display.

Bit 31 – Spare (stored in a register)

Bit 32 – Test bit

Used in some auto-tests.

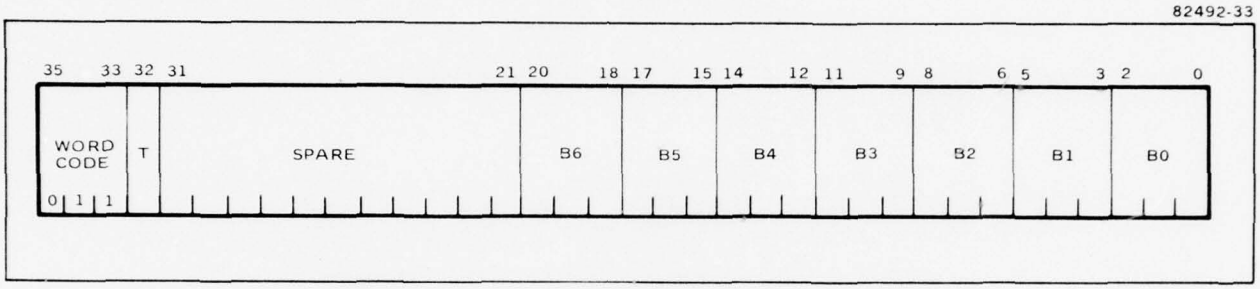
Bits 33-35 – Word Code

This code identifies the instruction type.

FORMAT OF BRIGHTNESS GROUP WORD

The brightness group word is used only in the display of time compressed sonar events.

Time Compression Brightness Group Word – The brightness group word is used only in the display of sonar events in a time compressed sequence. By appropriate coding of the B fields of the word, various visual effects may be created. This results from the intensity level of the events varying with time. See figure below. Refer to a later topic for a discussion of time compressed displays.



Time Compression Brightness Group Word Format

CODING OF TIME COMPRESSION BRIGHTNESS GROUP WORD

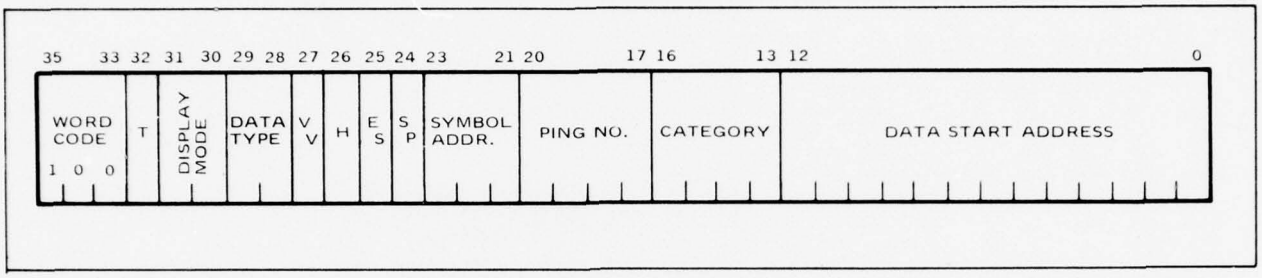
Bits 0 – 2	Brightness group B0 Brightness group code 2 1 0 Octal Intensity Level 0 0 0 0 0 – Blank Display 0 0 1 1 1 0 1 0 2 2 0 1 1 3 3 1 0 0 4 4 1 0 1 5 5 1 1 0 6 6 1 1 1 7 7 – Brightest Display
Bits 3 – 5	Brightness group B1
Bits 6 – 8	Brightness group B2
Bits 9 – 11	Brightness group B3
Bits 12 – 14	Brightness group B4
Bits 15 – 17	Brightness group B5
Bits 18 – 20	Brightness group B6
Bits 21 – 31	Spare
Bits 33 – 35	Word code The word code of 011 identifies the instruction as a brightness group word.

FORMAT OF DATA START/STOP WORD

The Data Start/Stop words retrieve a block of data from memory and control the display of this data.

Data Start Word – The data start word is used with a data stop word to retrieve from memory and control the dispiay of a block of data words, as shown below.

82492-34



Data Start Word Format

CODING DATA START WORD

Bits 0 – 12

Data Start Address

Binary Code, Bit 0 – LSB
Bit 12 – MSB

Bits 13 – 16

Category Code

16	15	14	13	
–	–	0	0	Category 1
–	–	0	1	2
–	–	1	0	3
–	–	1	1	4
0	0	–	–	1
0	1	–	–	2
1	0	–	–	3
1	1	–	–	4

Bits 17 – 20

Ping number

20	19	18	17	
0	0	0	0	Oldest Ping
0	0	0	1	Next Oldest Ping
.	.	.	.	
.	.	.	.	
.	.	.	.	
.	.	.	.	
1	1	1	1	

CODING DATA START WORD (Continued)

Bits 21 – 23 — Symbol address MSB's

23	22	21	Memory Address Decimal	Memory Address Octal
0	0	0	7168 - 7295	16000 - 16177
0	0	1	7296 - 7423	16200 - 16377
0	1	0	7424 - 7551	16400 - 16577
0	1	1	7552 - 7679	16600 - 16777
1	0	0	7680 - 7807	17000 - 17177
1	0	1	7808 - 7935	17200 - 17377
1	1	0	7936 - 8063	17400 - 17577
1	1	1	8064 - 8191	17600 - 17777

Bit 24 — Spare

Bit 25 — Expanded sector bit

ES = 0 Data is not expanded sector data
ES = 1 Data is to be displayed in the expanded sector

Bit 26 — Horizontal displacement bit

H = 0 Ignore horizontal displacement code
H = 1 Use horizontal displacement code

Bit 27 — Velocity vector bit

VV = 0 Not velocity vector
VV = 1 Velocity vector

Bits 28 – 29 — Data type code

29	28	
0	0	Forbidden
0	1	Events
1	0	Alphanumerics
1	1	Processed data symbols

Bits 30 – 31 — Display mode

31	30	
0	0	Single symbol display
0	1	Line type I display
1	0	Line type II display
1	1	In-line A-N display

Bit 32 — Test bit

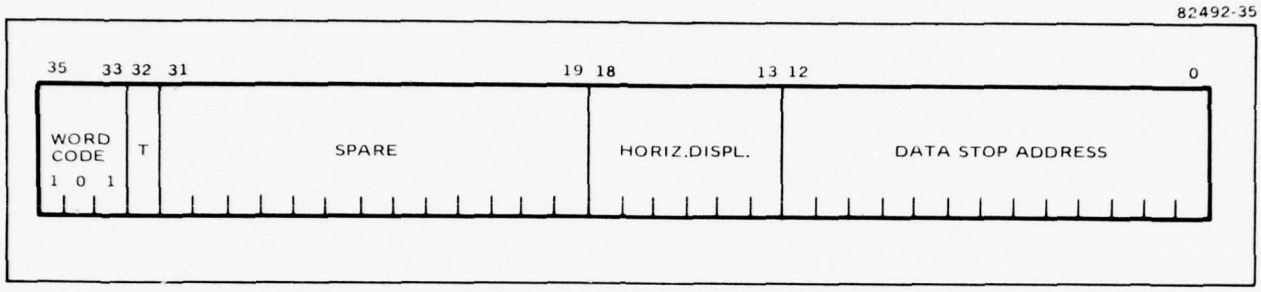
T = 0 Not test word
T = 1 Test word

Bits 33 – 35 — Word code

35	34	33	
1	0	0	Data start word

FORMAT OF DATA START/STOP WORD (Continued)

Data Stop Word – The data stop word is used to define the end of a block of display data words in the MMSC memory. Data stop words are always used in conjunction with a data start word. The horizontal displacement code for sonar events is specified in the word and the coding shown below.



Data Stop Word Format

CODING THE DATA STOP WORD

Bits 0 – 12	Data stop address (exclusive) Binary code, Bit 0 – LSB Bit 12 – MSB
Bits 13 – 18	Horizontal displacement code – sonar events Binary code, Bit 13 – LSB Bit 18 – MSB Bit 13 = 1 LSB of defl. = 0.015" Bit 14 = 2 LSB of defl. = 0.030" Bit 15 = 4 LSB of defl. = 0.060" Bit 16 = 8 LSB of defl. = 0.120" Bit 17 = 16 LSB of defl. = 0.240" Bit 18 = 32 LSB of defl. = 0.480"
Bits 19 – 31	Spare
Bit 32	Test bit
Bits 33 – 35	Word code 35 34 33 Data stop word 1 0 1

FORMAT OF POSITION WORD

The location of all symbols and line data is controlled by the position word.

There are four types of data words which provide detailed display information in an MMSC. The position word is described below. The Line Word, Alphanumeric Word and the symbol code words are described in the following topics.

Position words are used singly or with line or alphanumeric words for display of all symbols and line data. See figure on the opposite page.

The X and Y coordinate fields are transferred from the Memory Data Register to the X and Y Deflection Registers. The only manipulation of the coordinate data is for expanded sector display.

For In-Line alphanumerics the first A-N displayed will be located at the X and Y coordinates of the position word.

Each stroke in the symbol code word has its length specified as 1X, 2X, 3X, or 4X of the resolution given by bit 20. Thus if bit 20 is 0 the stroke lengths are: 0.020", 0.040", 0.060", or 0.080", if bit 20 is a 1 the corresponding stroke lengths are: 0.040", 0.080", 0.120" or 0.160".

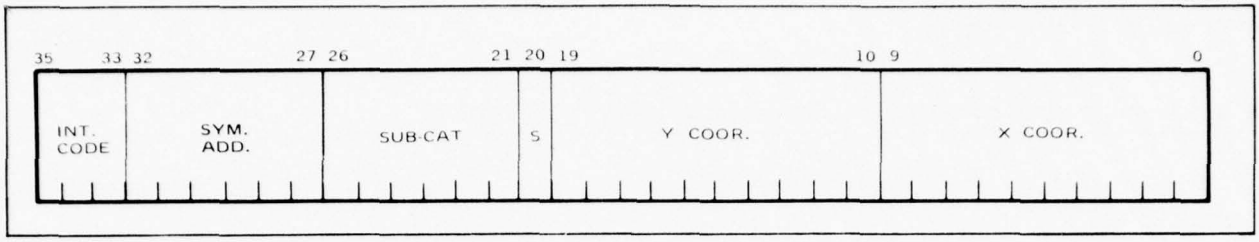
The subcategory code is used with the category code of the data start word by the console logic for comparison with the operator category select switches. There must be at least one 1 in bits 21-26 for the word to be recognized as a position word. Bits 21-23 specify the sub-category associated with category bits 13 and 14 of the data start word. Bits 24-26 are related to category bits 15 and 16 of the data start word.

The address LSB's of the first symbol code word of the symbol to be displayed is contained in bits 27-32. For non-processed data symbols and lines – Type II, bits 1 through 6 of the 13 required memory address bits are contained in the symbol address code. For processed data symbols bits 2 through 7 are contained in the symbol address code.

The intensity code field is used to intensify the symbol or line at a selected level. At the 50 F.P.S. frame rate and the operator intensity controls fully CW, intensity code 7 results in a symbol brightness of 25 ft-lamberts. The ratio in CRT brightness for any level to the next lower level is 1.65:1.

The coding is shown on the Table.

82492-36



Position Word Format

CODING THE POSITION WORD

Bits 0 – 9

X coordinate
Binary code, Bit 0 – LSB
Bit 9 – MSB
All "0"s = Left edge
All "1"s = Right edge

Bits 10 – 19

Y coordinate
Binary code, Bit 10 – LSB
Bit 19 – MSB
All "0"s = Bottom edge
All "1"s = Top edge

Bit 20

Symbol size
S = 0 = 0.020" stroke resolution
S = 1 = 0.040" stroke resolution

Bits 21 – 26

Sub-category code

26 25 24 / 23 22 21	Octal	
0 0 0	0	Forbidden code
0 0 1	1	Sub-category 1
0 1 0	2	2
0 1 1	3	3
1 0 0	4	4
1 0 1	5	5
1 1 0	6	Display
1 1 1	7	Inhibit display

Bits 27 – 32

Symbol Address Code Bit 27 LSB

Bits 33 – 35

Intensity code

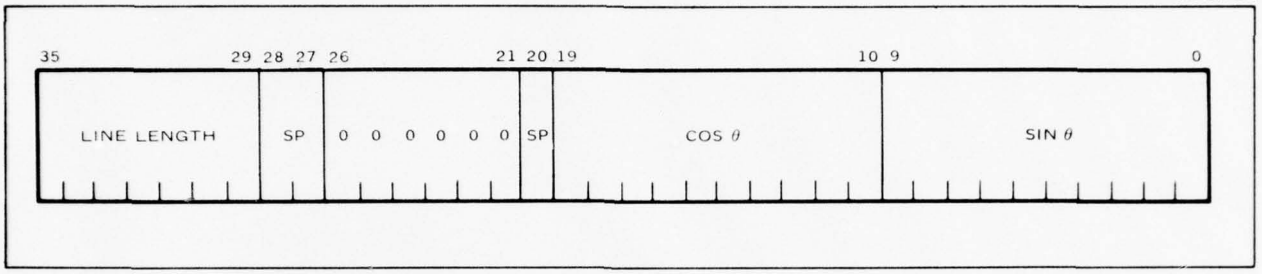
35 34 33	Octal	
0 0 0	0	Blank
0 0 1	1	Level 1
0 1 0	2	2
0 1 1	3	3
1 0 0	4	4
1 0 1	5	5
1 1 0	6	6
1 1 1	7	7 (brightest)

FORMAT OF LINE WORD

A line word is used to define the direction and length of a line.

The direction of the line is defined by the sin θ and cos θ bits. The length of the line is defined by the length code and the starting point is defined by the position word.

82492-26



Line Word Format

The values of sin θ (Bits 0-9) and cos θ (Bits 10-19) must be chosen such that $\sin^2\theta + \cos^2\theta = 1.0 \pm 0.004$ to insure accurate line scaling. The CRT beam velocity is controlled by the sine and cosine values and if by error the value of $\sin^2\theta + \cos^2\theta < 0.001$ the beam will be essentially motionless at some spot with a possibility of phosphor damage.

Bits 21 through 26 (the word code) must all be 0 in order that the display logic may differentiate between a position and a line word.

The length code (bits 29-35 determines line length by controlling the line intensity unblank time. Line display time is limited to 4 μsec which corresponds to 2 inches in line length.

The coding is shown in the table.

CODING OF LINE WORD

Bits 0 – 9

Sin θ Code

Bit	Value	Weight
0	0	-0.001
	1	+0.001
1	0	-0.002
	1	+0.002
2	0	-0.004
	1	+0.004
3	0	-0.008
	1	+0.008
4	0	-0.016
	1	+0.016
5	0	-0.031
	1	+0.031
6	0	-0.062
	1	+0.062
7	0	-0.125
	1	+0.125
8	0	-0.25
	1	+0.25
9	0	-0.5
	1	+0.5

Bits 10 – 19

Cos θ Code

Same bit weighting as the SIN θ CODE.

Bits 21 – 26

Word Code

26	25	24	23	22	21
0	0	0	0	0	0

Bit 27

Spare

Bit 28

Spare

Bits 29 – 35

Length Code
Binary Code
Bit 29 = 0.021"
Bit 30 = 0.042"
Bit 31 = 0.084"
Bit 32 = 0.168"
Bit 33 = 0.336
Bit 34 = 0.672
Bit 35 = 1.344
(MAXIMUM LENGTH IS 2.0")

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FORMAT OF ALPHANUMERIC WORD

Alphanumeric words are used with a position word to form an in-line alphanumeric display.

The alphanumeric word contains the symbol code word start addresses for four alphanumeric characters. See figure on the opposite page.

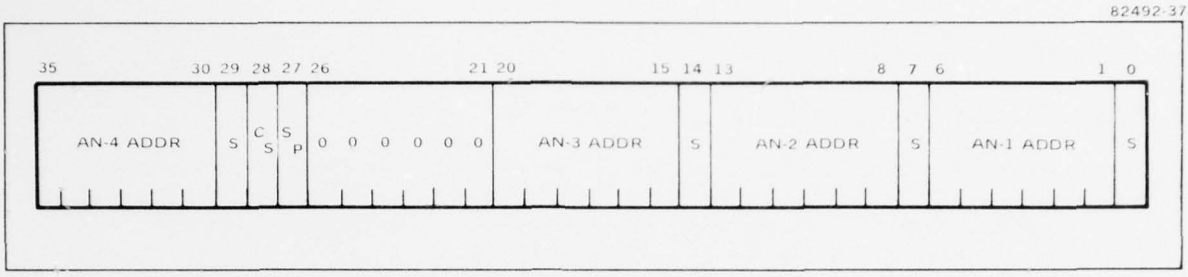
For a given alphanumeric, each stroke in the symbol code word has its length specified as 1X, 2X, 3X or 4X of the resolution given by bit 0, 7, 14 or 29 depending on the AN number.

The alphanumeric (AN) address code becomes bits 1 – 6 of the complete 13 bit symbol code word address. The AN address code is the start address of the symbol code words that define the AN character.

Bits 21 – 26 must all be 0 in order that the display logic can differentiate position words from alphanumeric words.

There are two options for the center-to-center horizontal spacing of in-line alphanumerics, 0.120 inch and 0.240 inch as specified by bit 28.

The coding is shown in the table.



Alphanumeric Word Format

CODING THE ALPHANUMERIC WORD

Bit 0	Character size AN-1 S = 0 = 0.020" Resolution S = 1 = 0.040" Resolution
Bits 2 – 6	AN-1 Address Code
Bit 7	Character Size AN-2: Refer to Bit 0
Bits 8 – 13	AN-2 Address Code
Bit 14	Character Size AN-3: Refer to Bits 2 – 6
Bits 15 – 20	AN-3 Address Code
Bits 21 – 26	Word Code 26 25 24 23 22 21 0 0 0 0 0 0
Bit 27	Spare
Bit 28	Character Space, 0 = 0.120" 1 = 0.240"
Bit 29	Character Size AN-4: Refer to Bit 0
Bits 30 – 35	AN-4 Address Code

FORMAT OF SYMBOL CODE WORD

MMSC symbols are composed of short line segments with variable length and direction and are defined by the Symbol Code Word.

Symbol code words define symbol shapes for the symbol generator. The MMSC symbols are composed of short line segments (strokes). The strokes are placed end to end to form a complete symbol. Strokes may be chosen to have any of 16 directions with 0^{o} being vertical and 90^{o} to the right.

The stroke length is variable and the resolution multiplier in the position or alphanumeric words defines the absolute stroke length values.

The blank bit is used to create dashed or discontinuous symbols. If less than 5 strokes of a symbol code word are necessary for a symbol the unused stroke codes must have a 0 in the blank bit.

The strokes are displayed in the sequence, stroke 1, stroke 2, stroke 3, stroke 4, and stroke 5.

The last symbol code word of a particular symbol must contain a 1 in bit 35 or the Symbol Address Counter will continue to increment and additional symbol code words will be read and displayed.

The symbol word coding is shown in the table.

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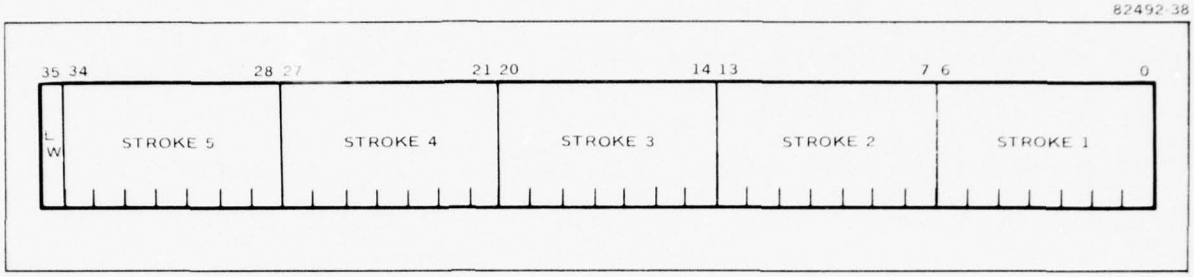


Symbol Code Word Format

CODING THE SYMBOL WORD

Bits 0 – 6	Stroke 1 Code								
	S_6	S_5	S_4	S_3	S_2	S_1	S_0		
	–	–		0	0	0	0	Stroke Direction	180^o
	–	–		0	0	0	1		90^o
	–	–		0	0	1	0		270^o
	–	–		0	0	1	1		0^o
	–	–		0	1	0	0		225^o
	–	–		0	1	0	1		135^o
	–	–		0	1	1	0		315^o
	–	–		0	1	1	1		45^o
	–	–		1	0	0	0		207^o
	–	–		1	0	0	1		117^o
	–	–		1	0	1	0		297^o
	–	–		1	0	1	1		27^o
	–	–		1	1	0	0		243^o
	–	–		1	1	0	1		153^o
	–	–		1	1	1	0		333^o
	–	–		1	1	1	1		63^o
	–	1	1			–		Stroke Length	1
	–	0	1			–			2
	–	0	0			–			3
	–	1	0			–			4
	0	–				–		Blank	
	1	–				–		Unblank	

Bits 7 – 13	Stroke 2 code
Bits 14 – 20	Stroke 3 code
Bits 21 – 27	Stroke 4 code
Bits 28 – 34	Stroke 5 code
Bit 35	LW = 0 = Not last symbol code word LW = 1 = Last symbol code word

DIRECTION AND LENGTH CODING FOR SYMBOLS

The length of strokes and the number of strokes for any symbol that is displayed is limited by the dynamic range of the symbol integrator and the cumulative position error.

Symbol Shape Coding – The design of a symbol shape and the generation of its required symbol code words will be facilitated by adhering to the guidelines and restrictions presented in this section.

Symbol Design Limitations – The maximum length per axis for any symbol using one position word is ± 3/8" (0.375). This requirement is imposed by the dynamic range of the symbol integrator.

Due to cumulative position error, use of more than 30 strokes for any symbol is not recommended. Symbols with larger numbers of strokes will tend not to "close", i.e. the last stroke's position will be in error by an amount proportional to the number of strokes and becomes noticable for large numbers of strokes.

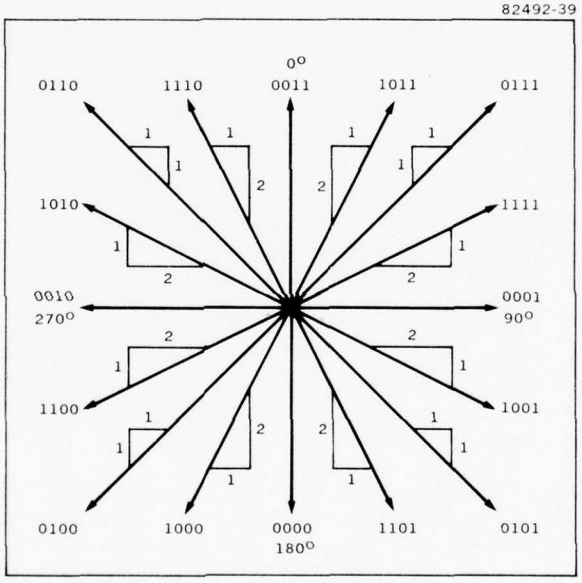
Stroke directions are the 16 given in the Table.

For symbols with the 0.040 in resolution multiplier the following length count restriction applies: The sum of the stroke length counts for a symbol must not exceed the quantity 12x no. of symbol code words read from memory.

Length Coding – Stroke lengths are specified on an axial basis. For stroke directions, 45^{o}, 135^{o}, 225^{o}, and 315^{o}, the X and Y components of direction are equal. For stroke directions 0^{o}, 90^{o}, 180^{o}, and 270^{o}, either X or Y component of direction is zero. For the above eight directions, one length count is required for each desired increment of X and Y movement. The increment of movement will be either 0.020" or 0.040" depending on the resolution multiplier. For the remaining eight stroke directions there is a two-to-one axial relationship as depicted in the figure. The length count specifies the longer component for these 27^{o} and 63^{o} strokes. The length counts are summarized in the Table.

LENGTH COUNT TABLE (0.020 RESOLUTION)

Stroke Direction		1		2		3		4	
0^{O}, 90^{O},	X	0 or 0.020"		0 or 0.040"		0 or 0.060"		0 or 0.080"	
180^{O}, 270^{O}	Y	0.020" or 0		0.040" or 0		0.060" or 0		0.080" or 0	
45^{O}, 135^{O},	X	0.020"		0.040"		0.060"		0.080"	
225^{O}, 315^{O},	Y	0.020"		0.040"		0.060"		0.080"	
27^{O}, 63^{O}, 117^{O}, 153^{O},	X	.010"	.020"	.020"	.040"	.030"	.060"	.040"	.080"
207^{O}, 243^{O}, 297^{O}, 333^{O}	Y	.020"	.010"	.040"	.020"	.060"	.030"	.080"	.040"



Stroke Direction Codes

DESIGN GUIDELINES FOR NUMERIC SYMBOLS

Guidelines and examples are given to show the process of programming highly legible numeric symbols with minimum strokes arranged in optimum sequence.

Symbol Design Guidelines – Two examples of numeric symbol shapes are given as aids in designing other symbols. The primary attribute of a well designed symbol is legibility under varied operating conditions. Symbol aesthetics and economy of strokes are important considerations in symbol display. Symbols should be designed on a grid of either 0.02 inches or 0.04 inches scale to facilitate coding. These remarks apply equally to alphanumeric or geometric symbols described in the succeeding topic.

Example 1 – The numeral 2 shown in Figure A is a straight forward design requiring 8 strokes. The use of 0.020 in. stroke segments indicates the resolution bit of position words and alphanumeric words would be required to be a "0" for this 0.080 in by 0.120 in. size. The symbol can be doubled in size by setting the resolution bit equal to "1". The representation given will differ from the displayed symbol in several ways. Line width is often overlooked when a sketch is prepared. Stroke 8 is scaled to 0.010 in. in width. The effects of line width are most pronounced for small closed symbols. The junctions between strokes of different orientation is a smooth curve. The CRT beam must be considered as having inertia. The wide bandwidth circuitry of the MMSC will limit overshoot for abrupt direction changes to less than 1/2 line width. The sum of the length counts for all 8 strokes is 17 which is less than 24 (12 x 2 symbol code words) allowable for 40 mil resolution display.

The detailed coding of the two symbol code words for the numeral 2 is given in Figure C. Note that the direction codes for strokes 9 and 10 are not all zero. The code for stroke 9 retraces the path of stroke 8. The stroke following the last displayed stroke should either retrace or continue in the same direction as the last stroke. This will preclude the possibility of a "tail" at the symbol termination due to misalignment of the intensity circuits. The code of stroke 10 returns the beam to the symbol origin. The important concept is that all five direction codes of a symbol word move the CRT beam in some manner, failure to account for strokes may cause the beam to exceed the ± 0.375 inch dynamic range of the integrators.

Example 2 – The numeral 5 as shown in Figure B, requires 10 strokes or 2 symbol code words. A total of 19 length counts are used which means the character may have either 0.020 inch resolution (shown) or 0.040 inch resolution. Strokes 6, 7, and 8 are curved to aid in distinguishing the 5 from an s. The detailed coding for the symbol code word is given in Figure D.

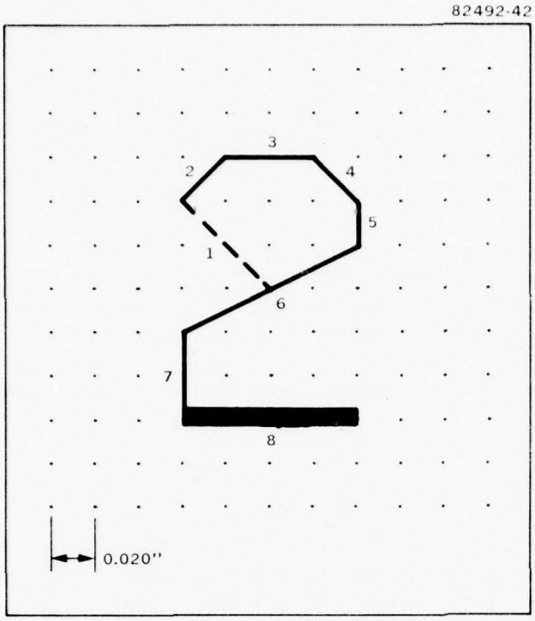


Figure A. Layout of the Symbol 2

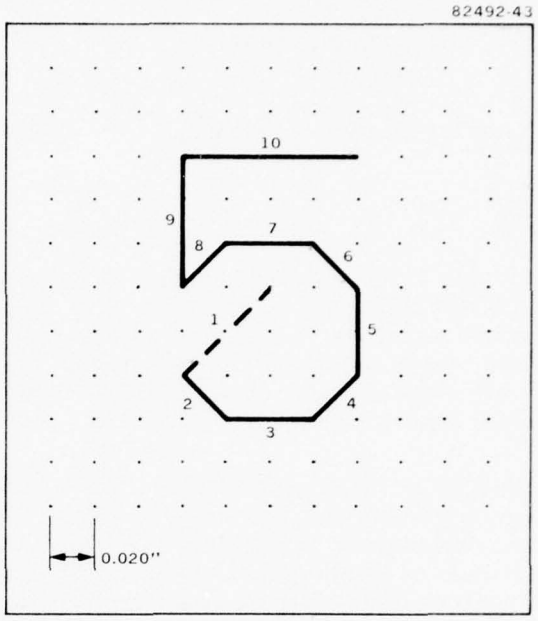


Figure B. Layout of the Symbol 5

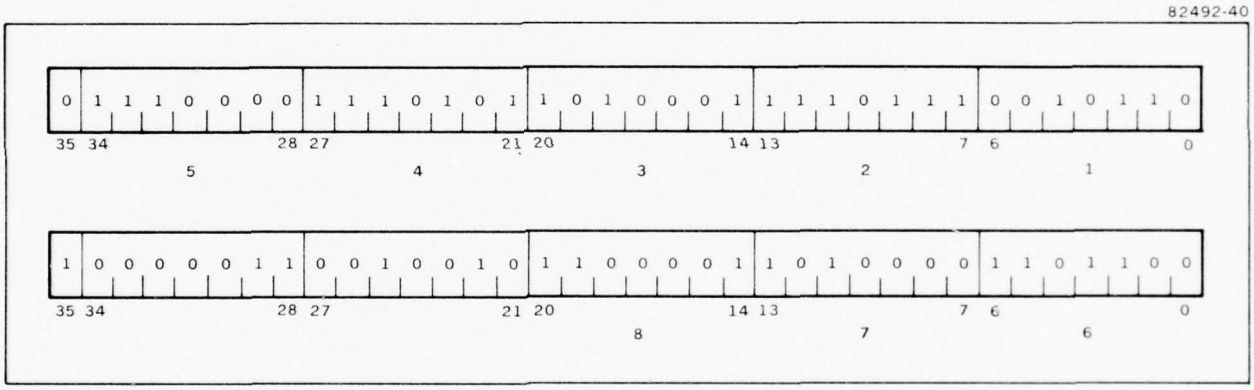


Figure C. Coding for the Symbol 2

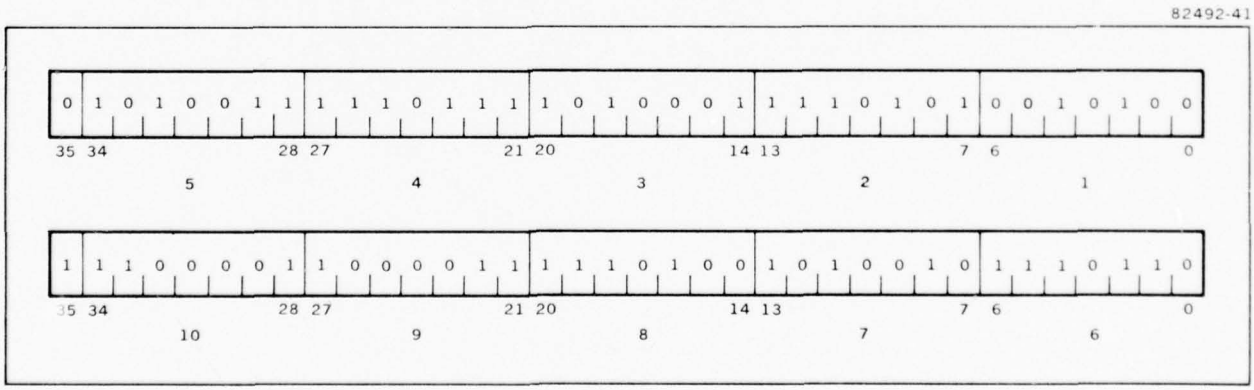


Figure D. Coding for the Symbol 5

DESIGN GUIDELINES FOR GEOMETRIC SYMBOLS

Two examples of geometric symbols are given and the method of programming is explained.

Example 1 – The processed data symbol of the Figure A below is an approximation of a quarter inch circle. The symbol is designed with 20 mil resolution to achieve smooth curved segments. As 19 strokes are required, 4 symbol code words must be coded. Since length code criteria is met, the same symbol code words may be used with the 40 mil resolution bit equal to "1" to display a 1/2 inch circle. See Figure D on the opposite page for coding.

Example 2 – Two approaches to the design of processed data symbol No. 2 are given in Figures B and C on the opposite page. The symbol was designed using 40 mil resolution. Sequence B is preferred over sequence A to minimize CRT beam "inertia" effects. The sum of length counts of the first eight strokes is 24 which indicates that for two symbol code words read from memory no time is available for strokes 9 and 10. A third symbol code word is required to allow display of strokes 9 and 10. This third word would have all unblank BITS set to "0" and the direction and length codes could be any arbitrary pattern. Strokes 9 and 10 would be coded in the second symbol code word.

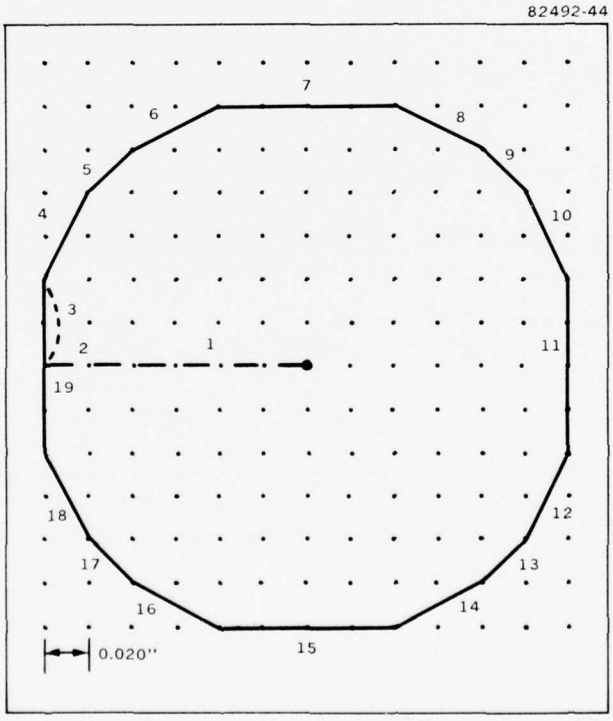


Figure A. Processed Data Symbol No. 1

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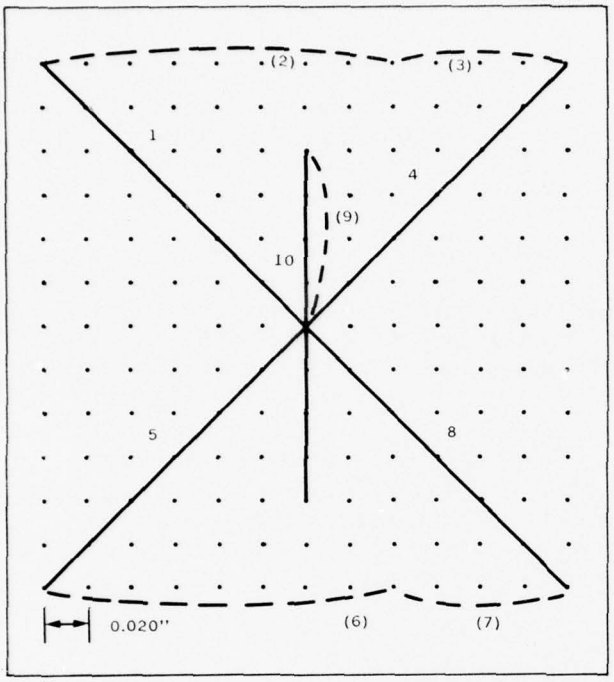

Figure B. Processed Data Symbol No. 2, Sequence A. Numbers in parenthesis ( ) indicate stroke blanked

82492-46

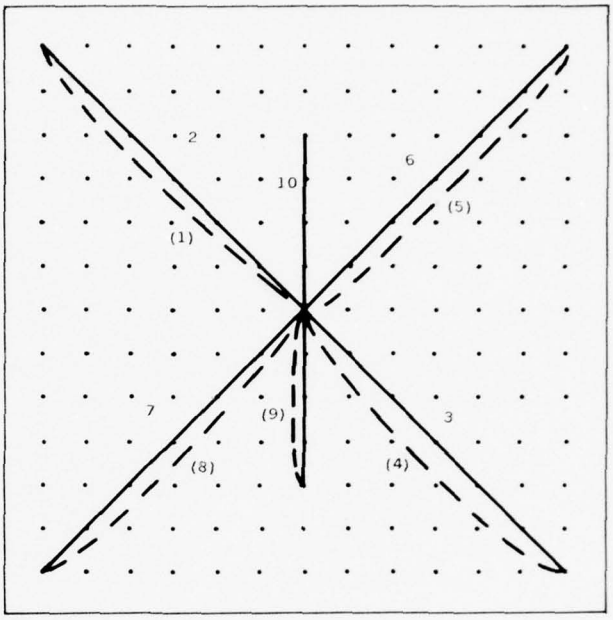

Figure C. Processed Data Symbol No. 2, Sequence B. Numbers in parenthesis ( ) indicate stroke blanked

82492-47

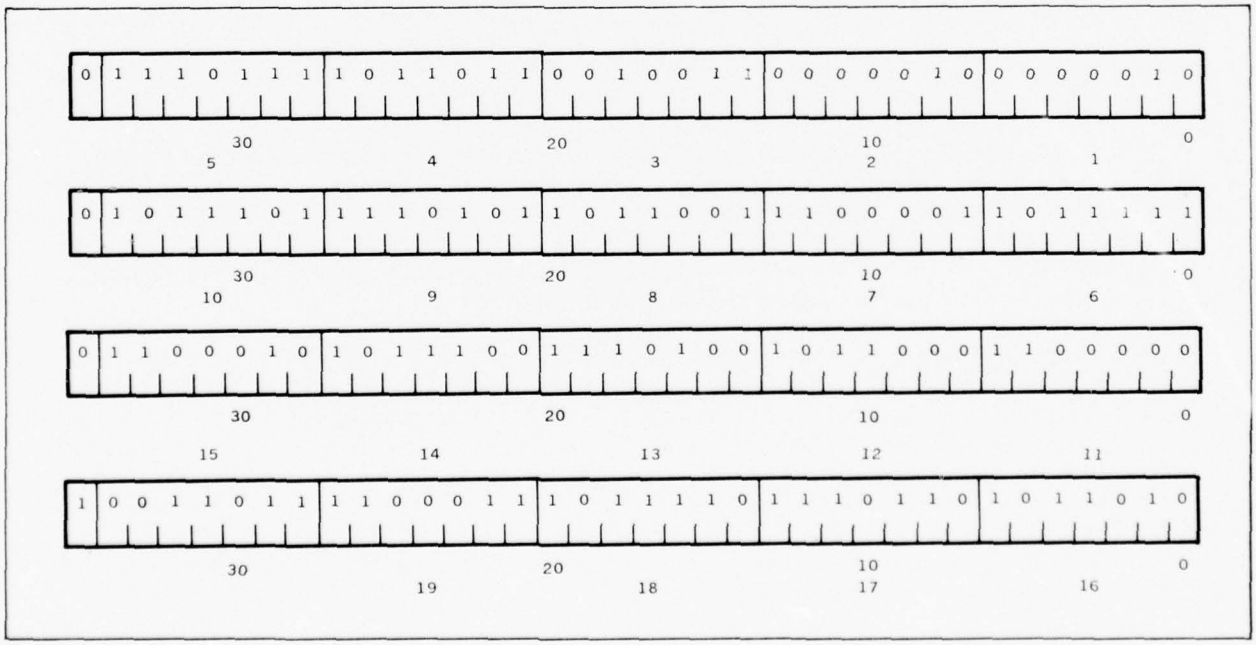

Figure D. Coding for Processed Data Symbol No. 1

DISPLAY OF LINES, IN-LINE ALPHANUMERIC AND PASSIVE DATA

Additional features of the MMSC include the display of lines, in-line alphanumerics and passive sonar data.

Line Display Generation – The MMSC can display line segments up to two inches in length. The number of lines presented each frame is limited only by the amount of symbols that must be displayed in a frame period. For line display only, 2500 lines may be displayed at the 50 Hz frame rate or 3500 at the 35 Hz frame rate.

Two data words stored in the MMSC memory define a line. A position word provides the start point, category, intensity, and for Type II lines, the memory location of the line word. The accompanying line word defines the line direction and length. The position word must always precede the line word. Position-line word pairs cannot be intermixed with the position words that define symbols. Separate data start-data stop instructions word pairs are required.

Line display time is 8 microseconds for any length line up to 2 in. Lines associated with track symbols may be designated as velocity vectors by setting bit 27 of the data start word. This action transfers control of the line brightness from the Lines brightness control to the Symbols brightness control. Sufficient length and angular resolution exists to permit connection of line segments to form grids, maps, graphs and long lines.

In-Line Alphanumerics – The in-line alphanumeric mode is particularly suited for display of alphanumerics to accompany track symbols or to present lines of text. A position word must precede any group of alphanumeric words. The position word establishes the coordinates of the first alpha character, and the intensity and subcategory of all in-line alphanumerics that follow until the next position word. In a block of display data defined by a data start-data stop instruction word pair there may be as many position words with following alphanumeric word(s) groups as desired.

Generation of a blank character such as occurs at the end of a sentence is accomplished by addressing a symbol code location that has the unblank bit for each stroke a "0".

Use of the keyboard on the MMSC to enter text on the display screen requires a program within the system computer as the keyboard does not directly enter data into MMSC memory. The computer program must take the keyboard interrupts it receives as keys are depressed and format them into position and alphanumeric words. Generation of a small marker for a cursor to indicate to the operator where the next character entered will be displayed is performed by the computer.

Passive Data Display – Display of passive sonar data from the PDMU is initiated by setting the P bit (bit 26) of the format control word. Display of the passive data takes precedence over memory data. The symbols, lines, and alphanumerics that are to accompany the passive data are displayed in each frame following the last line of passive display. In the passive mode all symbols are displayed at the 44 Hz PDMU frame rate. As display of the PDMU data may take nearly the entire display frame, the number of symbols displayed is limited. Refer to Appendix B for detailed timing limitations. Control of passive data formats, CRT placement, and number of bands and lines displayed is done with external function and instruction words to the PDMU from the computer.

HORIZONTAL-DISPLACEMENT AND EXPANDED-SECTOR DISPLAYS

The horizontal-displacement is available to separate closely spaced sonar events. The expanded-sector increases visibility in areas of crowded display by enlarging that sector.

Horizontal Displacement – The MMSC horizontal displacement feature is used with sonar events only and permits the operator to separate closely spaced events.

When the H bit (bit 26) of a data start instruction is "1" and the data type field specifies sonar events, the horizontal displacement field of the following data stop instruction is used to offset all the events specified by the instruction word pair, by a small amount in the -X (left) direction. No displacement occurs in the vertical direction. The amount of displacement from the X coordinate in each position word is the same for all events of an instruction pair. The scaling given in the data stop instruction description is for the operators panel Displacement control fully CW. As the Displacement control is rotated CCW the scaling is proportionately reduced. At full CCW the events will be displayed at the position word coordinates. The primary use of horizontal displacement is expected to be the display of ping history. The newest ping would have no horizontal displacement, the next oldest would have a small increment, the next oldest ping a greater increment, etc. By use of the operator control all pings may be displayed on the beam line or displaced. Horizontal displacement may be used with expanded sector and time compressed sonar event displays.

Expanded Sector – The expanded sector logic within the console permits repositioning data on the display by changing instruction words.

When the ES bit (bit 29) of the format control word is "1" the following occurs: each data start word read is examined for the state of its ES bit (bit 25), if "0" the X and Y coordinate msb's of each position word read are compared with the stored quadrant designator from the format control word. If the display data is in the ES quadrant it is blanked and not visible on the console CRT. If the display data is not in the ES quadrant the data is displayed. If the data start ES bit is "1" the X and Y MSB's in each position word are not used. The Quad bits of the format control word become the X (bit 28) and Y (bit 27) deflection MSB's and the data is displayed. The display logic eliminates all non-expanded sector symbols, events, line, etc from the designated quadrant and locates the expanded sector display data in the ES quadrant. Coding by the computer of the 9 LSB's of the X and Y coordinates in each position word determine the degree of expansion on the display. By careful use of two or more format control words more than one expanded sector quadrant may be designated. For expanded sector purposes, the quadrant for in-line alphanumerics is that of the line start position word. Expanded sector operation in no way effects passive data display.

OPERATIONS SEQUENCE IN DISPLAYING TIME-COMPRESSED PING HISTORY

A unique feature of the MMSC display is Time Compression of Ping history which allows several minutes of ping history to be displayed in a few hundred milliseconds.

Time-Compressed Ping History – The MMSC time compression capability permits control over display timing sequences with only a minimum of interaction with the system computer. This capability allows control over the time dimension, a capability usually not provided on other displays.

Time compression implies that data is displayed at a rate greater than the sonar ping rate. The MMSC will display several minutes of ping history in oldest to newest ping sequence in a few hundred milliseconds.

Ping Display Sequence – For time compressed ping history display up to 16 pings may be utilized. The MMSC can display nominally 2500 sonar events at the 50 Hz, frame rate or 3500 events at the 35 Hz frame rate, thus the number of pings must be weighed against the number of events per ping. A data start-data stop instruction word pair defines the events of each ping. The ping number field of the data start word is used to control ping display sequence over a time compression cycle. Ping number code "00" will be the first displayed, "01" the next, etc. Normally the oldest ping will have ping number 00. After a new ping's events have been loaded in MMSC memory all data start word ping numbers must be updated. For oldest-to-newest ping display sequence each update would require the ping numbers to be reduced by 1.

Within a given frame the ping sequence is determined by the order of instruction words. The frame ping sequence may be visually important for short time compression cycles. As both the longer term and individual display frame ping sequence are controlled by the computer, considerable flexibility exists to create varied visual effects.

Data in memory not identified as sonar events such as alphanumerics or processed data symbols will not be time compressed but will be displayed in a normal way each frame.

Time Compression Parameters – A single time compression cycle is diagrammed in the figure. It consists of a display period and the dwell period. The display period may be several seconds in duration. The dwell period is variable from 1 to 32 display frames and during this interval there is no display of any sonar events.

The display period is composed of up to 32 ping progression periods which in turn are 1 to 16 display frames in length. The frame period (or rate), ping progression period, display period, and dwell period are specified by the format control word.

The console contains a number of counters and comparators that act upon the time compression parameters in the following manner. During the first ping progression period of a time compression cycle, only that ping with ping number 00 is displayed. It alone is displayed for as many frames as make up the ping progression period. In the figure this would be six frames. Each event of the ping is displayed just once per display frame. During the second ping progression period both ping No. "00" and "01" are displayed. Similarly during the third ping progression period pings 00, 01, and 02 are displayed for the number of frames that make up the ping progression period. When

the number of ping progression periods equals the display period, (for the figure this would be ten) the dwell period is started and no events are displayed.

The computer also has the capability to vary the intensity levels of the events with tim to further enhance the time compression capability. The time compression brightness group word is used to specify the display brightness sequence of each ping. The intensity code field in each event position word is not used, refer to line B of the figure. The ping progression periods, tc, are numbered from 0 to 31 maximum and this is the B count. The number of B counts is specified in bits 11-15 of the format control word. For any ping the brightness group B: selected is: $i = B - P$ where i is a selected brightness group B_0, B_1, B_2, ..., B_i, ..., B_6. B is the current B count and P is the ping number. For $B - P < 0$ there is no display of the pings events. For $B - P > 6$ the brightness group selected is B_6. The B_i intensity code may be any one of the 8 levels. All events of a given ping are displayed at the same intensity level.

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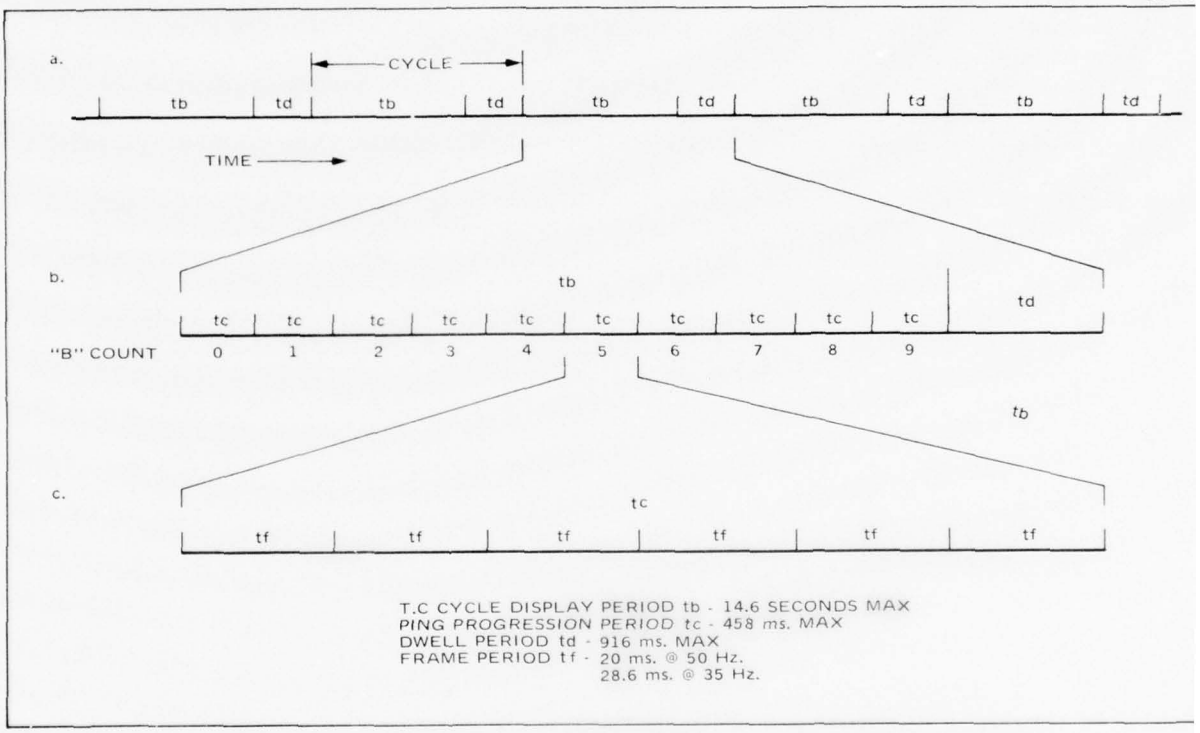


Operations Sequence in One Time-Compression Ping History

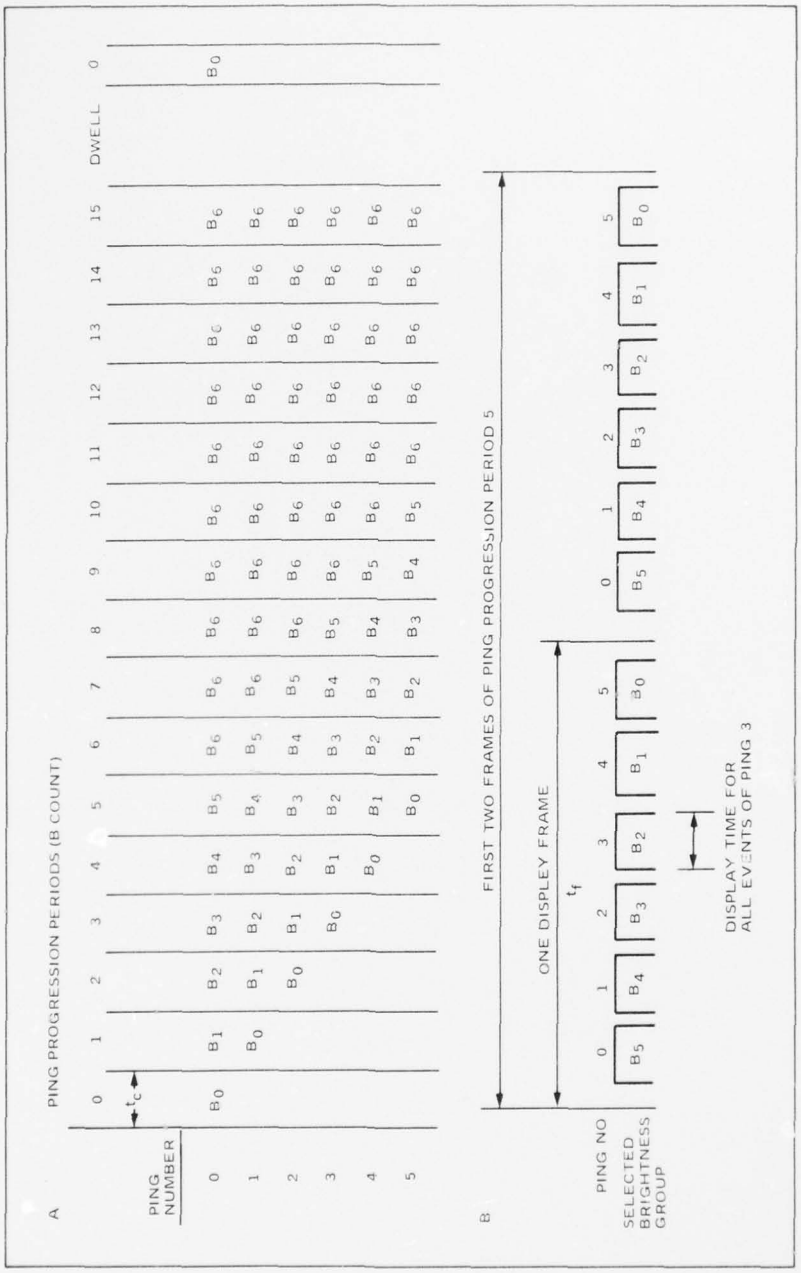
FACTORS IN ACHIEVING THE DESIRED BRIGHTNESS IN PING HISTORY

The control of brightness of the ping display allows variable CRT phosphor simulation in Time Compressed ping history. An example showing 6 pings is given and discussed.

An example is given for six pings in the figure. The brightness group selected for each ping's events is given as a function of the ping progression period. Part B of the example illustrates 2 frames of ping progression period 5. Assume brightness group Bo is coded 7 (maximum intensity), B1 = 6, B2 = 5, -, -, B6 = 1 and there are four frames per ping progression period (parameter C).

Ping Number 2, as an example, is not displayed during the 4 frames each of ping progression periods "0" and "1". During the four frames of period 2 the events of ping 2 are displayed at the Bo intensity level, 7. The next period ping 2 events are displayed at level 6 as the B1 code is selected. During ping progression periods 8 through 15 B6 is selected for ping 2. Each ping has the same sequence except they are staggered in time. Visually the events of each ping would be fully intensified then dimmed smoothly.

Visual Effects – Both the CRT phosphor and the observers eye will tend to integrate repeated excitations thus causing the number of frames/ping progression period (parameter C) to be as important as the brightness group in determining peak brightness. By appropriate brightness group coding, bright to dim, dim to bright, dim-bright-dim or uniform ping brightness profiles may be utilized for time compressed displays. The CRT phosphor used in the console decays to 1% of excitation brightness in 300 microseconds therefore one frame of dwell time is sufficient to achieve a dark display.



Brightness Control in Displaying Ping History. The figure shows six pings and the changes in brightness control.

SECTION 4
PDMU PROGRAMMING

Section 4 – PDMU Programming
Subsection – PDMU Functional Description

GENERAL PRINCIPLES OF OPERATION OF PASSIVE DATA MEMORY UNIT

The PDMU creates CRT beam-deflecting pulse trains in synchronism with intensity modulation signals to control the formation of BTR displays of passive sonar data on the MMSCs. Seven basic BTR formats are available.

The PDMU receives passive sonar data from the computer to use in generating BTR displays on the MMSCs. The passive sonar data is formatted by the computer into words composed of 3-bit intensity codes, with each 3-bit code representing the transient or time-averaged signal strength of one acoustic beam at some instant of time. The BTR displays are realized in the MMSC's by using the 3-bit codes to intensity-modulate a raster display. The PDMU transmits the intensity codes to the console along with the deflection pulse trains required to generate the raster.

The dimensions of the raster presented on the console's CRT are shown in the figure below. The display may be partitioned into a number of horizontal display bands separated by dark spaces (blank lines) to permit a number of time intervals to be displayed. The PDMU program words are used to control this function.

The PDMU can generate the BTR display in seven basic formats, with the computer controlling the format to be displayed. This is accomplished by the computer sending a passive format external function word to the PDMU with the desired format to be displayed. The display parameters for the seven formats are listed in the table on the facing page. The timing diagram of Figure B illustrates the timing of one line for each format. The "P" times of Figure B represents 2-microsecond memory cycle times. During the display portion of a line the memory is continuously accessed for display data, and only during the 8 μsec retrace interval is the memory available for I/O operations. The PDMU's Frame-Rate Generator causes the BTR display to be refreshed at the rate of 44 frames per second. At the time the frame start signal is set, the electron beam of an MMSC is at the lower left corner of the rectangular passive display area. The electron beam motion for display of passive data is from left to right and bottom to top.

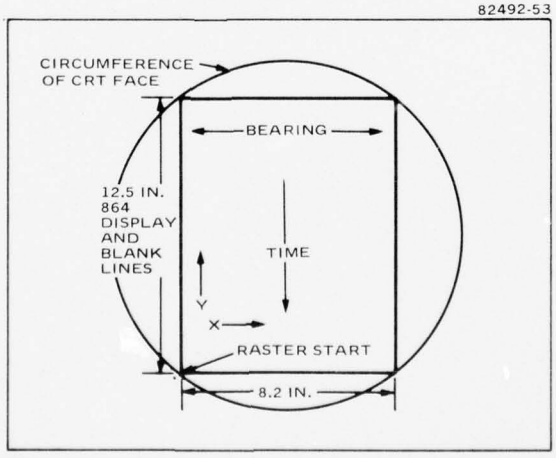


Figure A. Raster Dimensions for BTR Display of Passive Sonar Data on MMSC

DISPLAY PARAMETERS FOR SEVEN BTR FORMATS AVAILABLE FOR MMSC DISPLAY OF PASSIVE SONAR DATA

Format No.	Maximum Number of Lines Generated	Number of Beams Per Line	Number of Inten. Code Words/Line	Raster Width on MMSC Display (In.)	Displayed Beam Width (In.)	Display Position on MMSC
0	No Display					
1	680	144	12	8.2	0.058	Full Width
2	340	288	24	8.2	0.029	Full Width
3	680	144	12	4.1	0.029	Left Half
4	680	72	6	8.2	0.116	Full Width
5	680	72	6	8.2	0.116	Full Width
6	680	72	6	4.1	0.058	Left Half
7	680	72	6	4.1	0.058	Right Half

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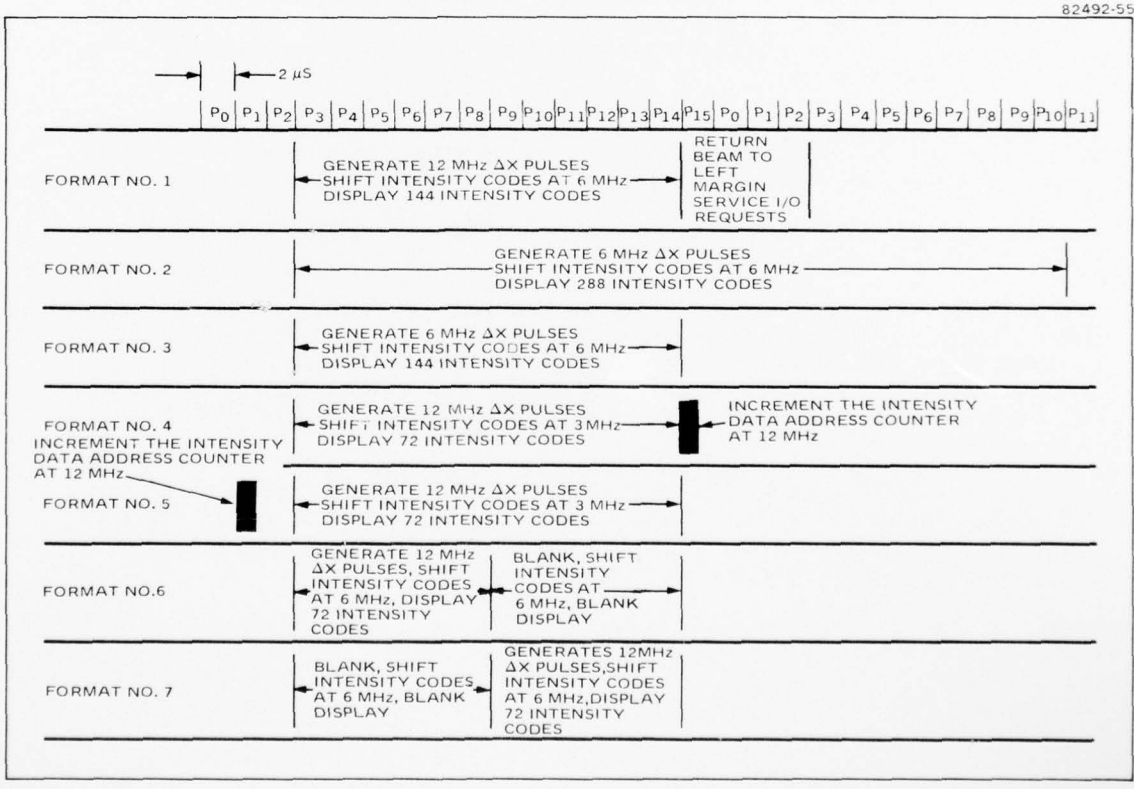


Figure B. Line Timing for One Line of Each BTR Display Format

PROGRAM-ACCESSIBLE PDMU UNITS INVOLVED IN GENERATING BTR DISPLAYS

The PDMU registers, counters, and logic that are directly utilized in generating the BTR display and are program accessible are described.

Format Register – The Format Register of the PDMU (see facing figure) is loaded upon receipt of a passive format external function word. The format defines the display parameters for the BTR presentation.

When power is first applied to the PDMU the Format Register is reset to format zero. In this format, three conditions are true: the PDMU is placed in the input/output mode, no BTR display data is generated, and every memory cycle is available for input/output operations with the computer. In this format the maximum data transfer rate between the computer and the PDMU can be accomplished. The computer can place the PDMU in the input/output mode at any time by simply sending a passive format external function with a format code of 0. When any of the other seven formats are sent to it, the PDMU will begin generation of the specified passive format at the completion of its current I/O operation.

Program Instruction Register – When a new program word is accessed from memory it is loaded into the Program Instruction Register. The new program word is stored in this register while the instruction type is being decoded and during the performance of the specified instruction.

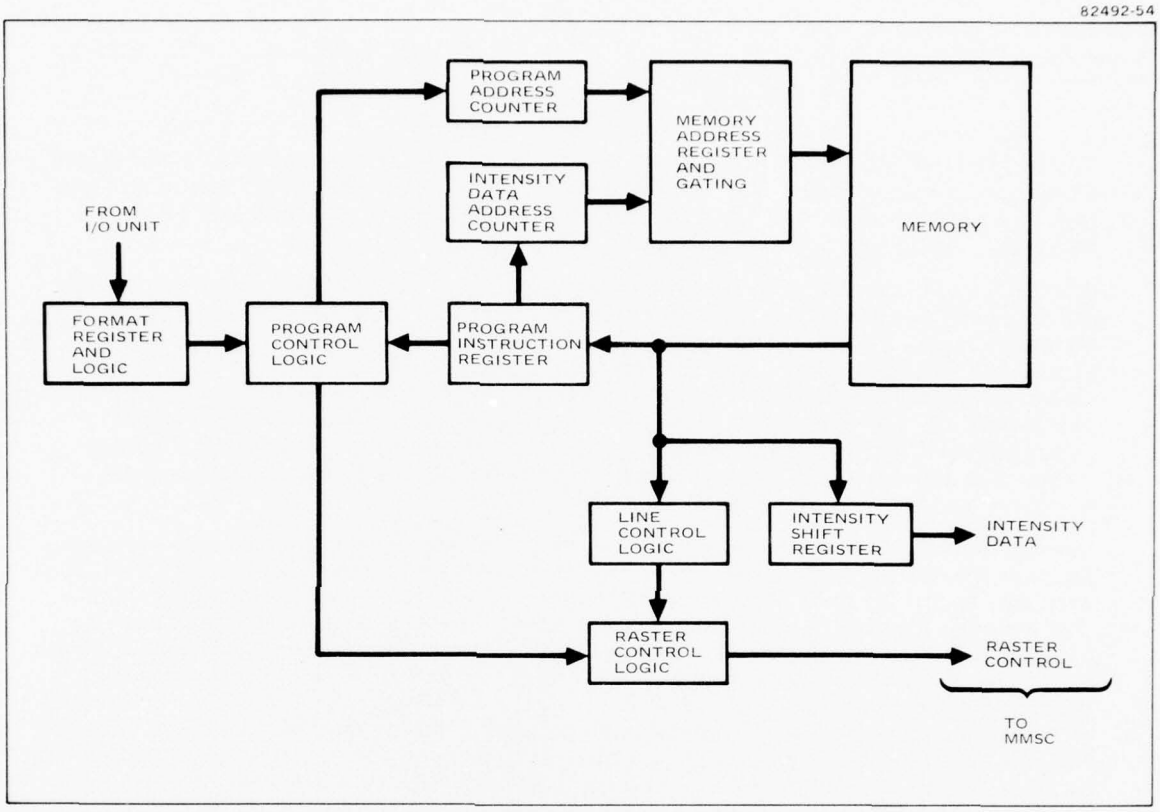
Intensity Data Address Counter – The Intensity Data Address Counter specifies the memory location from which the current intensity code word is being extracted. This counter is initially loaded from the Program Instruction Register.

Program Address Counter – The Program Address Counter specifies the memory location of the current program instruction word.

Memory Address Register – The Memory Address Register receives inputs from four address counters: the Input Data Address Counter, the Output Data Address Counter, the Intensity Data Address Counter and the Program Address Counter. The counter inputs are multiplexed into the Memory Address Register at the proper time, and the Memory Address Register holds the data for one memory cycle (2 μsec) while memory is being addressed.

Intensity Code Shift Register – The Intensity Code Shift Register performs a parallel-to-serial conversion of the intensity code words. During the display cycle, the intensity words are successively loaded into the shift register from memory and shifted out as twelve 3-bit codes in synchronism with the X deflection pulse train.

Line Control Logic – The Line Control Logic controls the positioning of information on the MMSC's display screen. From the Format Register, blank space information, and the line counter a sequence of X and Y deflection pulses are generated in synchronism with the shift rate of the intensity codes to create the passive display raster.



Functional Organization of Program-Accessible Units of PDMU That Are Directly Utilized in Generating BTR Displays

SEQUENCE OF PDMU OPERATIONS DURING BTR DISPLAY FRAME

The PDMU sequences its operations in a manner that achieves the required synchronism between deflection and intensity signals to create passive-sonar BTR displays on the MMSC's.

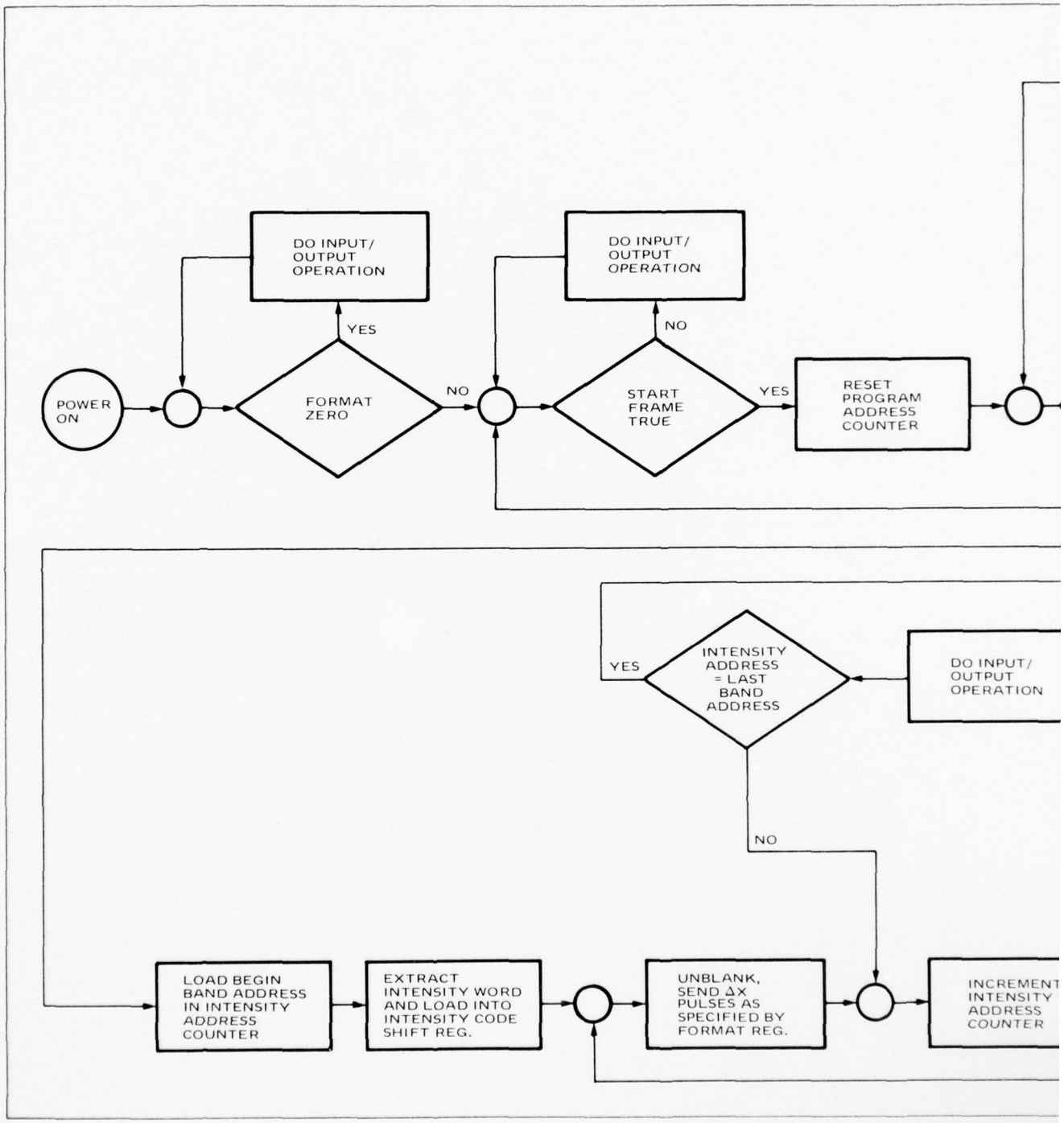
The sequence of PDMU operations during the BTR display frame is shown in the figure on the facing page. At the start of every frame the Program Address Counter is reset to all zeros; that memory location is accessed and the contents of memory location 00000 are loaded into the Program Instruction Register.

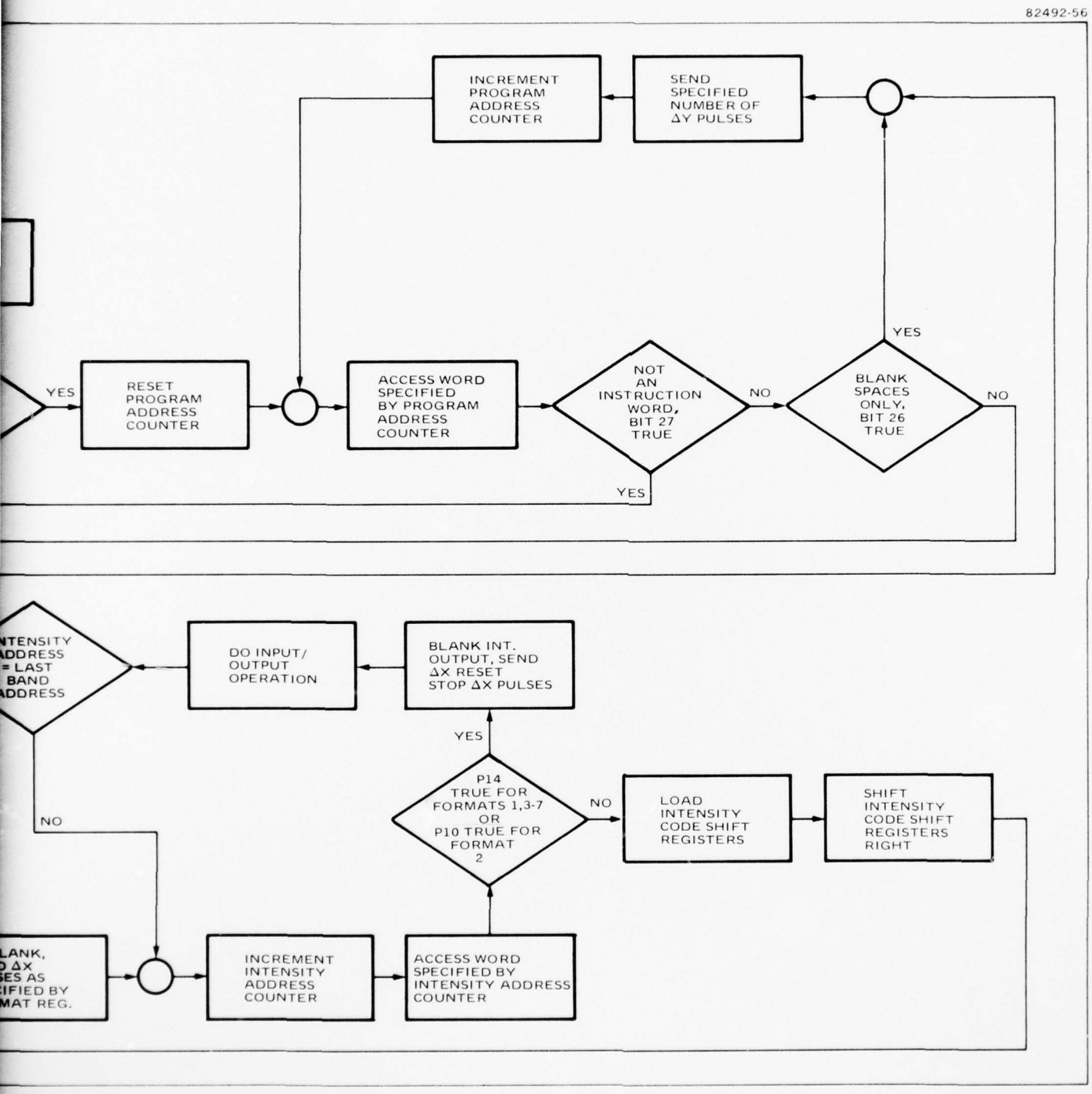
Three types of instruction words are recognized by the PDMU logic: blank spaces only (bit 26 true), not a valid instruction word (bit 27 true), or a valid instruction word (bits 26 and 27 false). If bit 27 is true the PDMU is ordered into the input/output mode until another start frame occurs, at which time the program counter is reset as described above. If blank-spaces-only (bit 26) is true the proper number of Δ Y deflection pulses is transmitted, the Program Address Counter is incremented and that instruction word is accessed. This instruction word is loaded into the Program Instruction Register where it is examined as indicated above. If bits 26 and 27 are both false the instruction word is assumed to be a valid instruction word.

When a valid instruction word is detected, bits 0-12 are loaded into the Intensity Data Address Counter and the PDMU is ordered into the display mode. The memory location specified by the Intensity Data Address Counter is accessed, and the data located in that memory location is loaded into the Intensity Code Shift Registers. The Intensity Code Shift Registers perform parallel-to-serial conversions of the intensity code words. Each intensity word contains twelve 3-bit codes and each 3-bit code represents one beam of intensity information (8 shades of gray). Bits 0-2 contain the three-bit intensity code for a beam, bits 3-5 contain the intensity code for the following beam, etc, and bits 33-35 contain the code for the last beam in that word. During the display cycle the intensity words are successively loaded into the shift registers and shifted out as twelve 3-bit codes in synchronism with the Δ X pulse train. As the PDMU causes the MMSC electron beam to move in a fixed raster pattern (for a given format), the computer must load the intensity words in a PDMU's memory in a prescribed manner in order to achieve the desired display (see page 4-8 for details). Twelve consecutive intensity words (24 for format 2) are required to define a horizontal raster line. A number of 12-word lines become a band with the first displayed band always defined by the first valid instruction word, the second band defined by the second valid instruction word, etc.

After each intensity word is accessed from memory, the Intensity Data Address Counter is incremented. This loading and incrementing continues until the Intensity Data Address Counter compares with that of bits 13-25 of the Program Instruction Register. When exact comparison occurs the line counter is incremented the number of counts specified by bits 28-35 of the Program Instruction Register. After incrementing is completed a new instruction word is accessed and loaded into the Program Instruction Register. This procedure is continued until the program counter reaches a not-valid-instruction word, causing the PDMU to go into the input/output mode until another start frame occurs.

The Program Address Counter is sometimes used in auto-testing. When the PDMU receives certain auto-test commands, program address 00037 must have been previously loaded with an auto-test word. This requires that program address 00036 must contain the not-valid-instruction-word bit set.

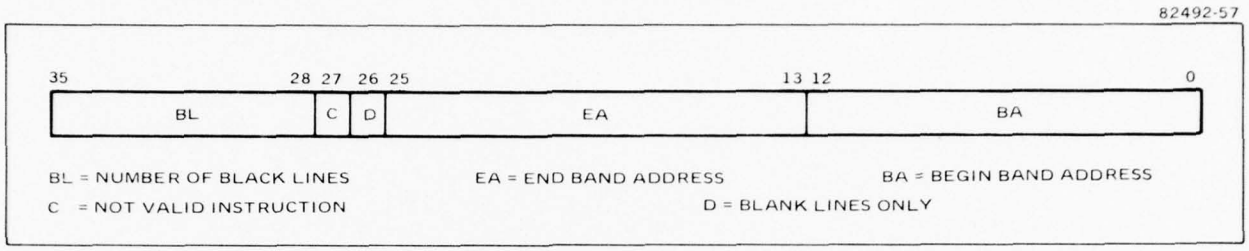

POWER ON
FORMAT ZERO
YES
DO INPUT/ OUTPUT OPERATION
NO
START FRAME TRUE
YES
DO INPUT/ OUTPUT OPERATION
NO
RESET PROGRAM ADDRESS COUNTER
INTENSITY ADDRESS = LAST BAND ADDRESS
YES
DO INPUT/ OUTPUT OPERATION
NO
LOAD BEGIN BAND ADDRESS IN INTENSITY ADDRESS COUNTER
EXTRACT INTENSITY WORD AND LOAD INTO INTENSITY CODE SHIFT REG.
UNBLANK, SEND ΔX PULSES AS SPECIFIED BY FORMAT REG.
INCREMENT INTENSITY ADDRESS COUNTER



PDMU's Sequence of Operations for BTR Display Frame

FORMAT OF PDMU INSTRUCTION WORD

The PDMU instruction words, stored in memory locations 00000 through 00037, are used to control band updating, band height, band spacing or positioning, and to optimize the data rate between the Computer and PDMU.



Format of PDMU Instruction Word

Bits 0-12, Begin Band Address (BA) – BA is given in binary code with bit 0 being the LSB. The begin band address is the memory location of the first intensity code word of the display band. The Intensity Address Counter is preset with bits 0-12.

Addresses 00000 through 00037 are reserved for instruction words and should not be coded in this field unless bits 26 or 27 are set to 1.

Bits 13-25, End Band Address (EA) – EA is in binary code, with bit 13 being the LSB. The Intensity Counter increments from the begin band address through the end address to define a display band. The end band address must always be numerically greater than the begin band address unless bit 26 or 27 is set to 1.

Bit 26 Blank Lines Only (D) – Bit 26=1 causes the BA and EA fields to be ignored. The raster will be moved up along the left margin by the amount specified in the blank line field (BL).

Bit 27, Not Valid Instruction (C) – For normal Display, bit 27 is 0 and the BA, EA and BL fields are used in the passive display generation. In the memory location following the last valid instruction, bit 27 must be set. This inhibits the Intensity and Program Counters from incrementing for the remainder of the display frame. Both bits 26 and 27 are to be set to 0 in an instruction word.

Bits 28-35, Number of Blank Lines (BL) – BL is in binary code with bit 28 being the LSB. Each binary count has a weight of 0.014 in. The blank lines are generated for a valid instruction word (bits 26 and 27 = 0) after the end band address is reached, i.e., the blank lines are above the displayed band.

If the BL field is set to zero for a valid instruction word, the first line of the next band will be superimposed over the last line of the previous band.

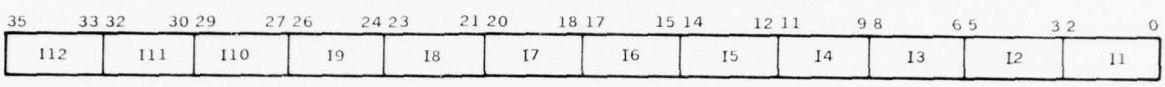
For blank lines only, the raster is incremented vertically with no display along the left passive display margin. The blank-lines-only instruction is primarily useful in establishing a lower margin above the normal raster start point.

Instruction Execution Time – Valid-instruction execution times are variable in time duration as a function of the number of lines of intensity data in a band. Each line of a Format 2 line takes 64 μs., and all other display formats take 32 μs. per line. A blank-lines-only instruction requires one line time to execute regardless of the BL field code.

FORMAT OF PDMU INTENSITY WORD

The PDMU intensity words, each containing twelve 3-bit codes of passive sonar intensity data, are stored in memory addresses 00040 through 17777. The words are retrieved from memory under control of the PDMU instruction words, then the codes are extracted from the intensity words and transmitted to the MMSC's for BTR display generation.

82492-58



IN EACH INTENSITY FIELD, OCTAL CODING IS USED WITH THE LSB BEING THE LOWEST BIT NUMBER: THE OCTAL CODING IS AS FOLLOWS:

OCTAL CODE	INTENSITY MEANING
0	BLANK DISPLAY
1	INTENSITY LEVEL 1
2	INTENSITY LEVEL 2
3	INTENSITY LEVEL 3
4	INTENSITY LEVEL 4
5	INTENSITY LEVEL 5
6	INTENSITY LEVEL 6
7	INTENSITY LEVEL 7

Format of PDMU Intensity Word

Each I field controls the MMSC's CRT display intensity (brightness) for a short length of a horizontal raster line. Code 0 results in a blank (dark) display and the level 7 code results in the brightest display of approximately 22 foot-lamberts. The I field codes are used in an MMSC to present eight shades of gray. The eight brightness levels are uniform over the face of the CRT to present a high-quality display. The I fields are transmitted to an MMSC in sequence beginning with I 1 and ending with I 12. The resulting CRT intensity sequence is from left to right.

Twelve intensity words (24 for format 2) define the display of a single raster line. The ordering of intensity words within a band determines the beam display location relative to the left margin and the lower edge of the band. The line display sequence is from CRT bottom to top.

The instruction word addressing permits the block of intensity words that define a band to be located anywhere in the intensity word store of memory.

USING PDMU WORDS TO GENERATE STATIC BTR DISPLAYS

Format examples are given to illustrate how PDMU instructions and intensity words are created to generate a static BTR display on the MMSC.

The PDMU-generated displays may be categorized as either static or dynamic: A static display does not change in real time, and a dynamic display is periodically updated by the computer (typical BTR display). Programming is somewhat different for the two cases, so the cases are separately described in this topic and the succeeding topic.

Operations using the static display involve changing the data base only infrequently and then an entire band at a time. Assume the PDMU contains instructions and intensity words that are to be superceded with a new display pattern. The computer transmits a passive format external function with format 0 specified (refer to example EXT-1 of Figure A). Format 0 stops the display and allows maximum computer-to-PDMU data transfer rate, once a memory load start has been sent. This operation is optional. If a lower data rate is tolerable, the computer may only send a memory load start external function (refer to example EXT-2 of Figure A).

The assembled intensity code words are transmitted to the PDMU via output acknowledge (OA) word-pairs. The first OA word specifies the PDMU memory address of the first intensity word of the display band. (Refer to examples INT-1, INT-2, INT-3, INT-4 of Figure B.) The intensity code words should be arranged in memory for either format 1 or format 2; i.e. for either 12 or 24 intensity words to form one line. The computer sends an instruction word via an output acknowledge word pair to specify begin band address, end band address and blank lines (refer to examples INSTR-1, INSTR-2 of Figure C.) The computer now sends an external function specifying the display format. Refer to example EXT-3 of Figure A). This initiates the desired display.

The use of format 0 is indicated as optional because it has both advantages and disadvantages. If a new band is to be added to the display of existing bands and momentary blanking of the passive display is undesired, the format 0 external function would not be used.

The instruction words illustrated in Figure C define a display of 100 lines of 144 beams full width across the MMSC display screen. The instruction word is specified (INSTR-1) to be stored in address 00000 which will cause this band to be the first to be displayed each frame, thus, placing it at the bottom of the display. The blank line code in INST-1 establishes a separation of 18 times 0.014 inch (approximately 0.25 inch) between the top edge (last line) of this band and the lower edge (first line) of the next band. The instruction word defining the next display band (no examples given) would be stored in address 00001.

The intensity words given as examples are located arbitrarily in locations 00040 through 02317, the lower 1200 cells of intensity word store. The first 12 intensity words define line 1, words 13-24 define line 2, which is displayed above line 1, etc. The location of a band of intensity words in memory in no way influences the vertical band location of the display. The order of readout of instruction words establishes band display sequence. The I field of the intensity word examples (INT-1, INT-2, INT-3, INT-4) contains an arbitrarily increasing-decreasing code pattern for beams 1-24 of the first line.

The format may be changed to any other except format 2 by sending one passive format external function. In formats 4 through 7 the PDMU logic assumes that the intensity code words were originally entered for format 1 display and it automatically skips 6 intensity code words each line.

If the format and valid instruction words are sent before the intensity data is loaded, the entering of this data will be observed on the display.

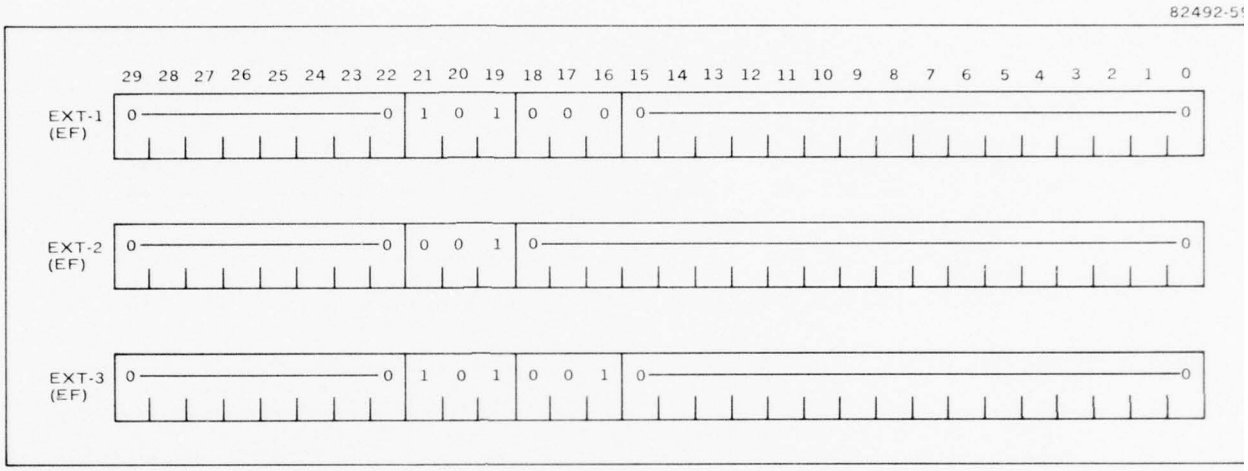


Figure A. External Function Words to Create Rasters for Passive Display. Example EXT-1 indicates passive format O, blanking the display and permitting maximum computer-to-PDMU data transfer. Example EXT-2 is a memory load start command. Example EXT-3 specifies passive format 1 for 680 lines, 144 beams full width.

USING PDMU WORDS TO GENERATE STATIC BTR DISPLAYS (Continued)

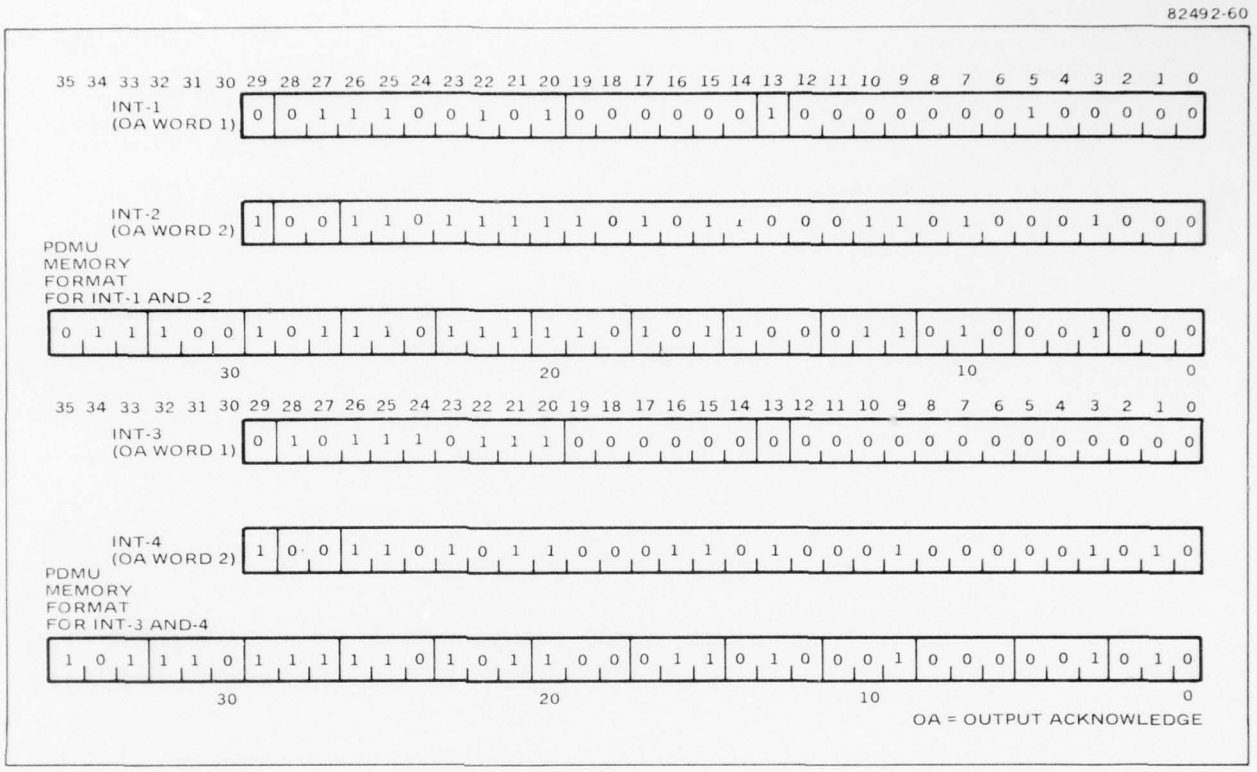


Figure B. Formation of PDMU Intensity Words. Bits 20 through 28 of INT-1 become bits 27 through 35 of the PDMU word, and bits 0 through 26 of INT-2 become bits 0 through 26 of the PDMU word. The new 36-bit word is stored in PDMU memory location 00040 (octal) as specified by bits 0 through 12 of INT-1.

AD-A043 817 HUGHES AIRCRAFT CO FULLERTON CALIF F/G 17/1
SOFTWARE MEMO FOR THE MULTIMODE SONAR CONSOLE DISPLAY SYSTEM. V--ETC(U)
AUG 68 N00123-67-C-0833
UNCLASSIFIED FR-68-11-653 NL

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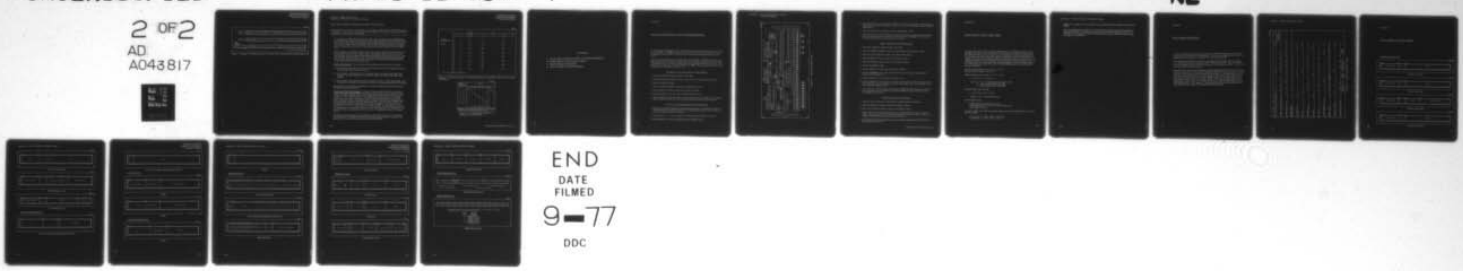

END
DATE
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DDC

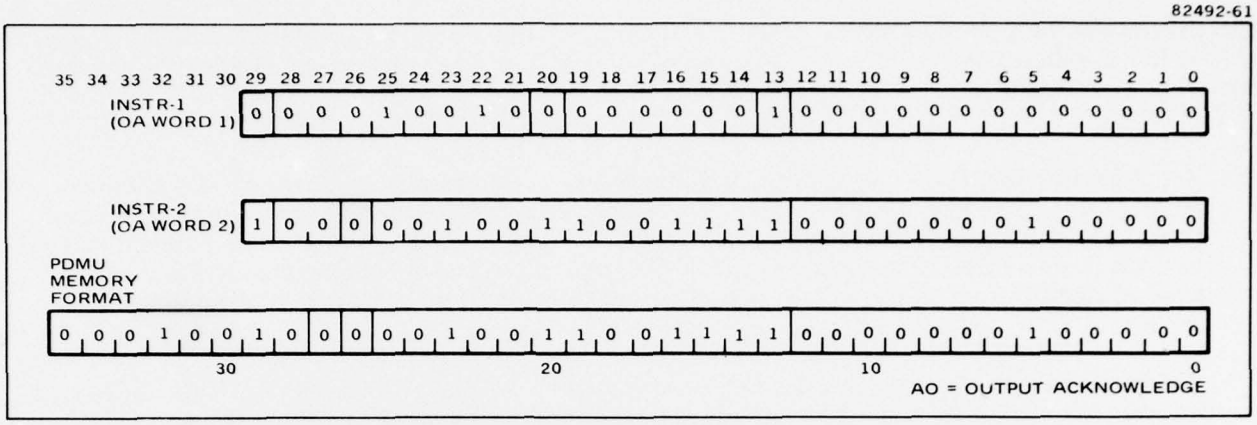

Figure C. Formation of PDMU Instruction Word from Two Computer Output Acknowledge Words.

USING PDMU WORDS TO GENERATE DYNAMIC BTR DISPLAYS

The generation of a passive sonar display to give a dynamic BTR representation of the sonar surveillance volume is the primary function of the PDMU. The computer controls the time dimension (Y or vertical axis) of the display.

Proper entry of PDMU Instruction and intensity words creates a dynamic BTR Display on an MMSC that smoothly moves (down or up) without blanking the entire display at any time. The memory-addressing technique used allows intensity words to be entered and remain at one PDMU memory address. The procedure for initial loading of a complete band of display data is the same as that described for static displays in the preceding topic.

The procedure for updating a display band a line at a time with the newest data replacing the oldest line in memory is given below. The display band will have the newest line displayed at the top edge and the oldest line displayed at the lower edge. The visual effect for this display sequence will be a downward movement of data at a rate proportional to the rate of entry of new lines. The effect will simulate the Bearing Time Recorder display seen in many sonar systems.

PDMU Band Updating – The procedure for band updating involves three main steps:

(1) The computer must have previously set the memory load FF by sending the memory load start external function command.

(2) The computer transmits one line of intensity words via output acknowledge. The intensity words are addressed to replace the oldest line of data of the band being updated.

(3) The computer then transmits two new instruction words via output acknowledge. The instruction words shall be addressed to replace the existing instructions for that band.

The rationale for requiring two instruction per passive display band is best explained through the example given below.

Example of PDMU Band Updating – Consider a passive display band of 6 raster lines, with 25 blank lines between this band and the band just above it. Each raster line is to contain 12 words of intensity data. The intensity data for the band is stored in memory location 101-172. The newest line is to be displayed at the top of the band, and the oldest line on the bottom. The passive band is essentially divided into two separate bands, although no gap appears between the two bands. This will allow updating a band by changing only one line of intensity data and the two instruction words. This is illustrated in the instruction update sequence shown in Figure A. The sequence of display is line 6, 5, 4, 3, 2, and 1 where 1 is the newest line of sonar data and 6 the oldest; this sequence is illustrated in Figure B. The requirement of two instruction words per display and a last instruction with bit 27 set to 1 establishes a limit of 15 display bands.

The passive display geometry on the MMSC will allow 864 lines (total) of both display and blank lines. If the PDMU instructions are such that this number is exceeded, the display will be driven off the upper edge of the MMSC's CRT.

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		35 — BL	28	27	26	25 — EA	13	12 — BA	0
ORIGINAL INSTRUCTIONS	1	1	C	0	D	0	172		101
	2	25		0		1	—		—
UPDATE 1	1	1		0		0	172		113
	2	25		0		0	112		101
2	1	1		0		0	172		125
	2	25		0		0	124		101
3	1	1		0		0	172		137
	2	25		0		0	136		101
4	1	1		0		0	172		149
	2	25		0		0	148		101
5	1	1		0		0	172		161
	2	25		0		0	160		101
6	1	1		0		0	172		101
	2	25		0		1	160		101
7	1	1		0		0	172		113
	2	25		0		0	112		101

NOTE: ALL NUMBERS ARE DECIMAL

Figure A. Example Showing How Two Instruction Words are Updated to Update an Entire Band of BTR Data

82492-63

INTENSITY WORD ADDRESSES	UPDATE 0	1	2	3	4	5	6	7
	CONTROLLED BY SECOND INSTRU.							
101 - 112	6	1	2	3	4	5	6	1
113 - 124	5	6	1	2	3	4	5	6
125 - 136	4	5	6	1	2	3	4	5
137 - 148	3	4	5	6	1	2	3	4
149 - 160	2	3	4	5	6	1	2	3
161 - 172	1	2	3	4	5	6	1	2
	CONTROLLED BY FIRST INSTRU.							

NUMBERS 1 - 6 INDICATE LINE NUMBER WITH 1 INDICATING NEWEST LINE AND 6 INDICATING OLDEST LINE

Figure B. Example Showing Sequence of Updating Lines of BTR Data

APPENDICES

A. USE OF THE MAINTENANCE PANEL IN PROGRAM DEBUGGING

B. PASSIVE DISPLAY LINES/SYMBOL TIMING

C. SINGLE SYMBOL MODE TIMING

D. TABLE OF MMSC AND PDMU FORMATS

Appendix A

USE OF THE MAINTENANCE PANEL IN PROGRAM DEBUGGING

By utilizing the maintenance panel, data may be entered or extracted one word at a time from an MMSC's or PDMU's memory. This feature can be effectively used in program debugging and fault isolation. Procedures for entering and extracting data are given below.

There are three procedures for entering data into an MMSC or PDMU. Two of the procedures simulate the computer output words. These are the external function and output acknowledge words. The third procedure allows a simplified direct memory input. The procedures are the same for both the MMSC and PDMU. The maintenance panel controls referred to are illustrated in Figure A-1.

EXTERNAL FUNCTION SIMULATE PROCEDURE

1. Set the ON LINE/OFF LINE switch to OFF LINE.
2. Place the MAINT CONTROL selector on the 30 BIT position (on-line simulate).
3. Depress MASTER CLEAR.
4. Place the CLOCK SELECT switch at the FREE RUN position.
5. Select IN REG for display on the 36 bit register readout.
6. Set bit switches 0-29 to the desired external function word.
7. Depress EXT FNC. The bit pattern on bits 0-26 of the 36 bit register readout should agree with bit switches 0-26. The external function word has now been entered.

OUTPUT ACKNOWLEDGE SIMULATE PROCEDURE

1. Observe the MEM LD indicator on the maintenance panel. If the Memory Load F/F is not set (indicator dark) send the memory load external function word by using the External Function Simulate Procedure.
2. Perform steps 1, 2, 4, and 5 listed for External Function Simulate Procedure.
3. Set bit switches 0-29 to the desired output acknowledge word 1.

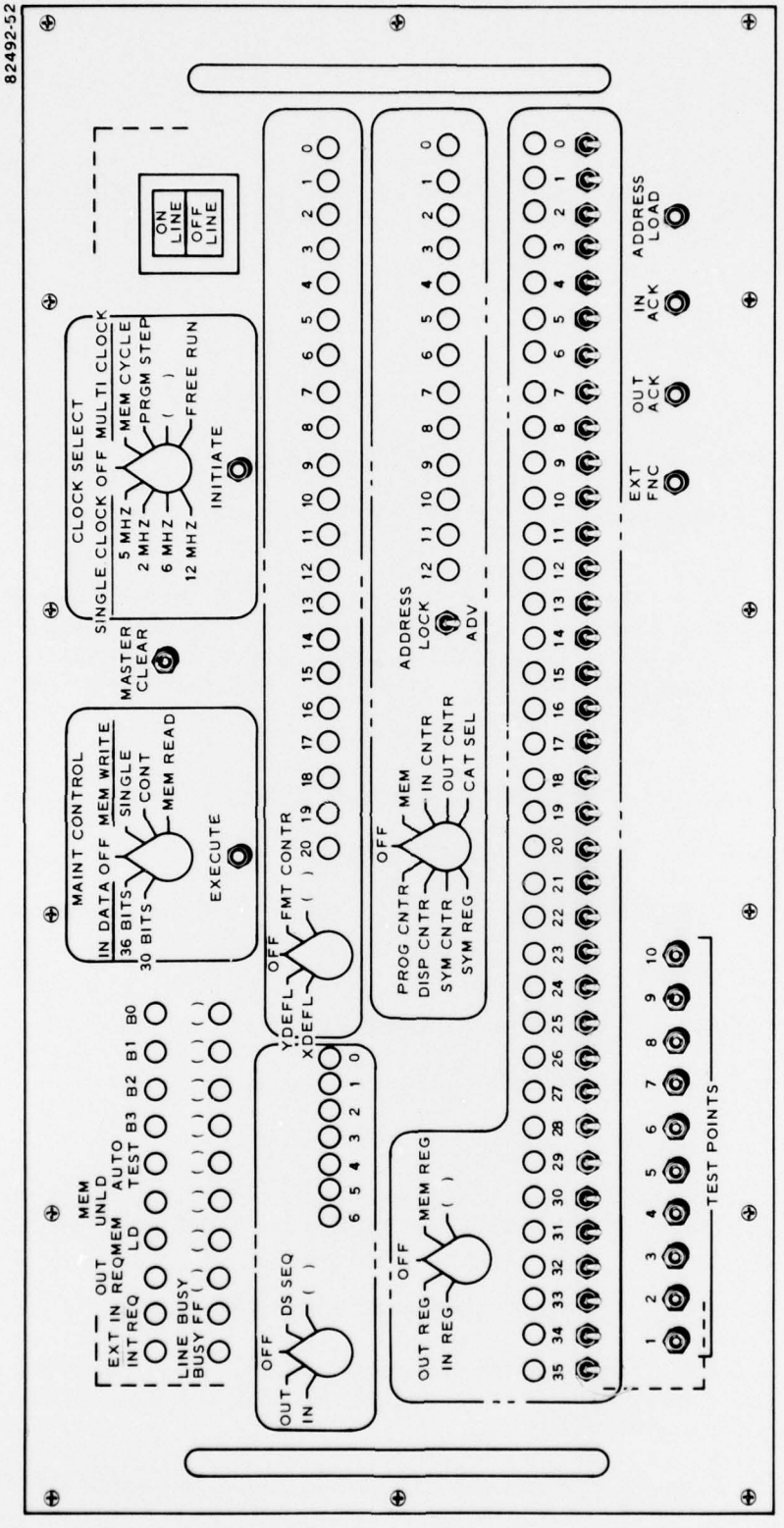


Figure A-1. MMSC Maintenance Panel

4. Depress OUT ACK. The bit pattern on bits 0-26 of the 36 bit register readout should agree with bit switches 0 through 26. Bits 27 through 35 should agree with bit switches 20 through 28.

5. Set bit switches 0-29 to the desired output acknowledge word 2.

6. Depress OUT ACK. The bit pattern on bits 0-26 of the 36 bit register readout should agree with bit switches 0-26. Bits 27-35 should remain unchanged. The word has now been entered into the desired memory location.

DIRECT MEMORY LOAD PROCEDURE

1. Set the ON LINE/OFF LINE switch to OFF LINE.

2. Place the MAINT CONTROL selector on the 36 BIT position (memory load).

3. Place the CLOCK SELECT switch at the FREE RUN position.

4. Select IN REG for display on the 36 bit register readout.

5. Select IN CNTR for display on the 13 bit register readout.

6. Depress MASTER CLEAR.

7. Set bit switches 0-12 to the desired memory address.

8. Depress ADDRESS LOAD. The bit pattern of the 13 bit register readout should agree with bit switches 0-12.

9. Set bit switches 0-35 to the desired memory word.

10. Depress EXECUTE. The memory word has now been entered. The bit pattern of the 36 bit register readout should agree with the bit switches. The 13 bit register readout will be incremented by one.

11. From this step, each successive depression of EXECUTE will load the bit switches into successive memory addresses. The Input Address Counter increments with each EXECUTE operation.

MEMORY READOUT PROCEDURE

1. Perform steps 1 through 4 of the External Function Simulate Procedure.

2. Select OUT REG for display on the 36 bit register readout.

3. Select OUT CNTR for display on the 13 bit register readout.

4. Send a memory unload external function word with the desired memory output address. The memory word will now appear on the 36 bit register readout. The 13 bit register readout displays the memory output address.

5. If consecutive memory addresses are to be read out, depress the IN ACK twice for each word to be read out.

BLANK PAGE FOLLOWS A-3/A-4

Appendix B

PASSIVE DISPLAY LINES/SYMBOL TIMING

Symbolic data such as track symbols, alphanumerics, and reference marks may be displayed with passive data on the MMSC. Such symbols are defined by words within the MMSC memory as are any other symbols. The display of such symbols and lines is restricted to the time at the end of the passive display frame. For a full passive display of 680 lines (340 for format 2) there is only time to display a few symbols. The equations that follow allow computation of symbol display time in the passive mode. If a large number of symbols and lines must be displayed in a passive mode, the number of lines of passive sonar data must be reduced sufficiently to remain within the system's capability.

Passive display frame time: 22,400 ± 0.01% μs.
Minimum symbol display time: 64 μs.

Passive display time, formats: 1, 3, 4, 5, 6 and 7.

$$T = 32\ \mu s\ (A + B + C) + 96\ \mu s.$$

where: A = No. of "blank lines" instruction words
B = No. of valid instruction words
C = Total display lines of all bands

Passive display time, format 2

$$T = 64\ \mu s\ (A + B + C) + 96\ \mu s.$$

where: A, B, C are as given above.

Symbol display time:

MMSC instruction readout time: 4 μs.
Symbol display time: 4 μs + 2 μs/symbol code word
Line display time: 8 μs.

A passive display of 4 bands of 660 lines total in format 1 would allow 928 μs. For display of symbols.

$$T = 32\ \mu s\ (0 + 8 + 660) + 96\ \mu s \approx 21,472\ \mu s.$$
Symbol time = 22,400 - 21472 ≈ 928 μs.

Thus 92 15 – stroke (10 μsec) symbols may be displayed with the passive format on the MMSC.

Once symbol display is started it is not stopped until all the programmed symbols and lines are displayed. If an operator requests more symbols than there is frame time available, part of the first band will not be displayed, giving a feedback indicator that the display is overloaded.

Appendix C

SINGLE SYMBOL MODE TIMING

To fully understand the operations performed in an MMSC during symbol/line display the basic display timing must be understood. To give some insight into the timing, the single symbol mode display is presented here as a typical example.

A simplified timing diagram for display in the single symbol mode is given in Figure C-1. The timing shown is primarily memory address associated. The abbreviations on the line labeled "Memory Enable" indicate the word type being read out – P for position word, SC for symbol code word.

Illustrated is a memory input operation with each displayed symbol. Choice of memory input was arbitrary as the one memory cycle per symbol for I/O unit use may be either a memory input (write) or memory output (read) operation. When the console has been instructed to simultaneously block unload and load, the memory control logic may receive both a memory input and a memory output request. In the single symbol mode, input requests have priority over output requests. In the line modes and the in-line alphanumeric modes there is no priority as both an I/O input and output may occur for each displayed line or AN character. The timing for lines and in-line alphanumerics is not given as these modes are variations of the basic timing.

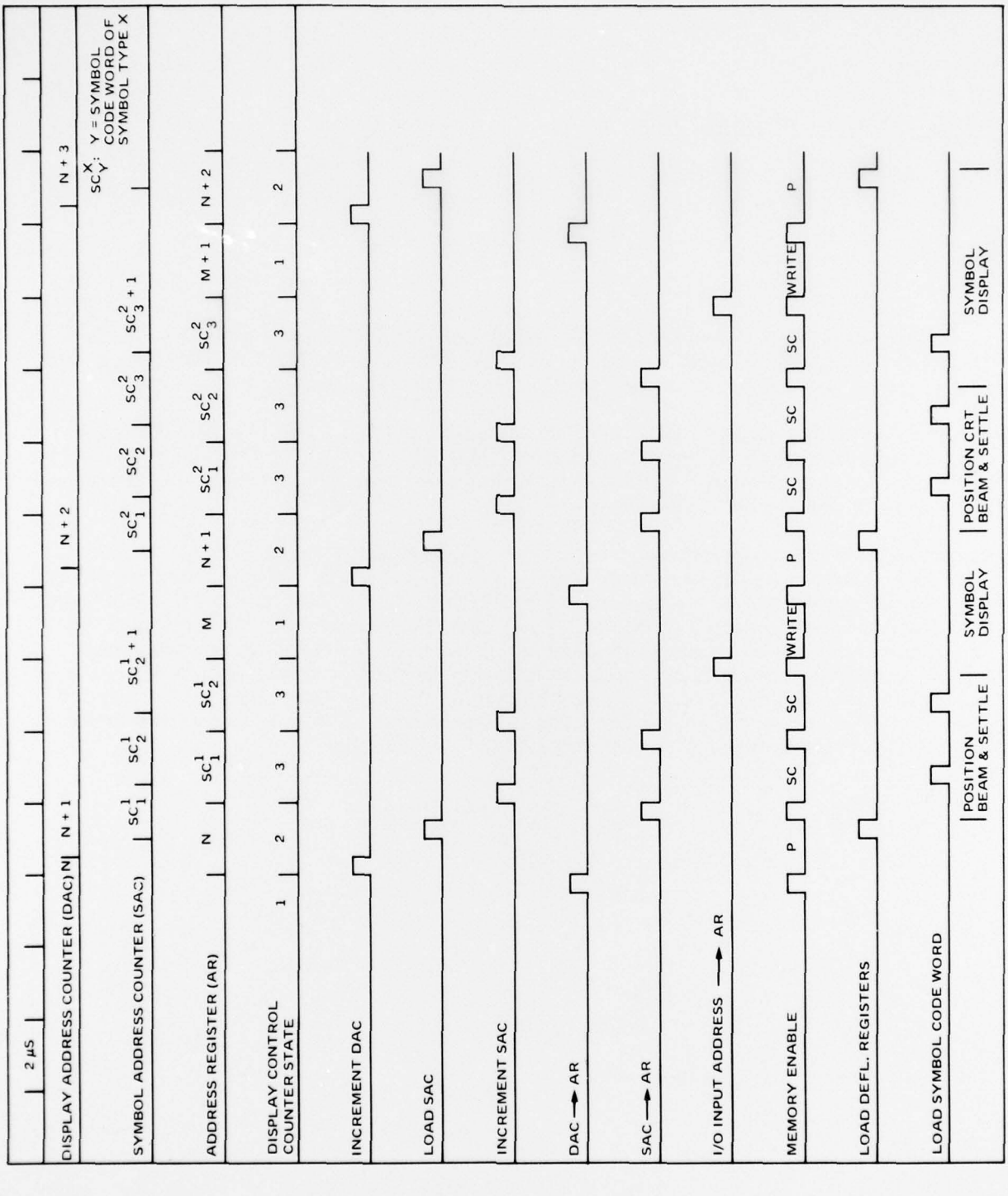


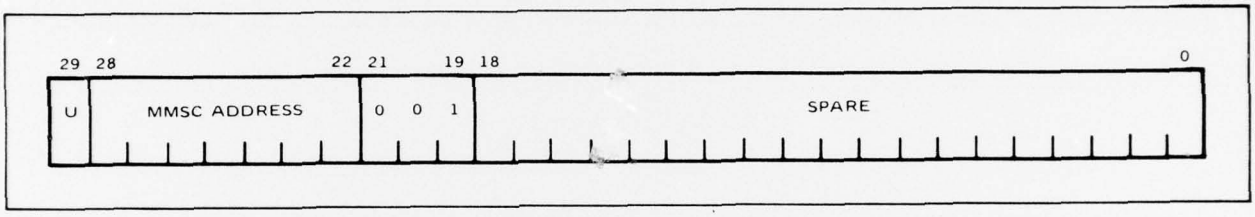
Figure C-1. Single Symbol Mode Timing

Appendix D

TABLE OF MMSC AND PDMU FORMATS

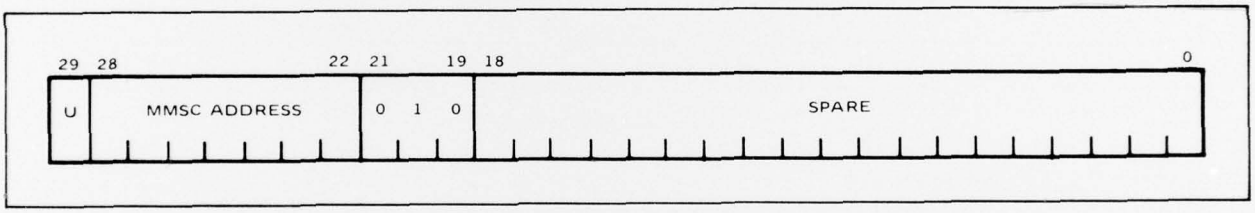
External Function Words

82492-5



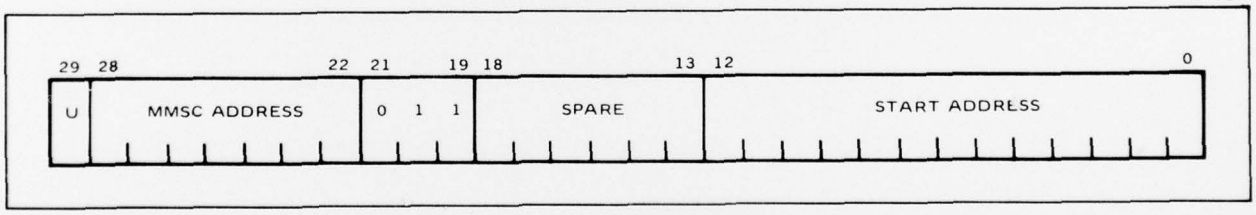
Memory Load Start

82492-6



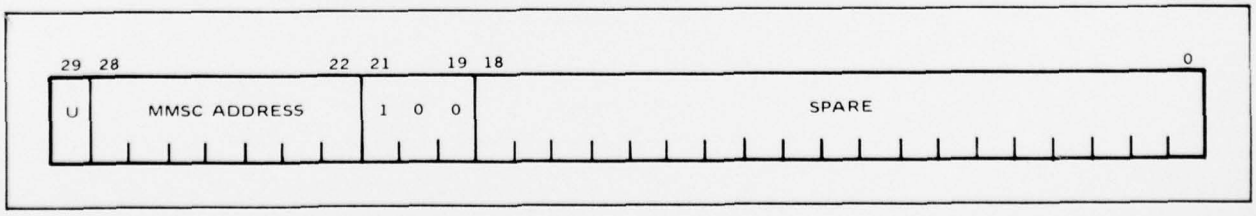
Memory Load Stop

82492-7



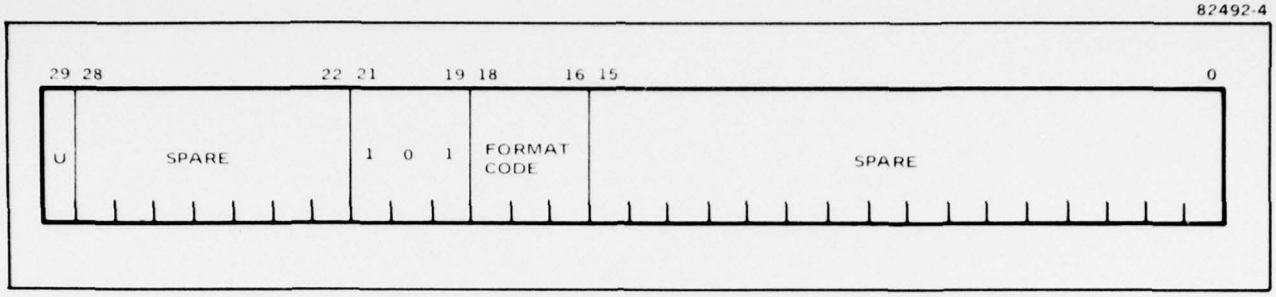
Memory Unload Start

82492-8



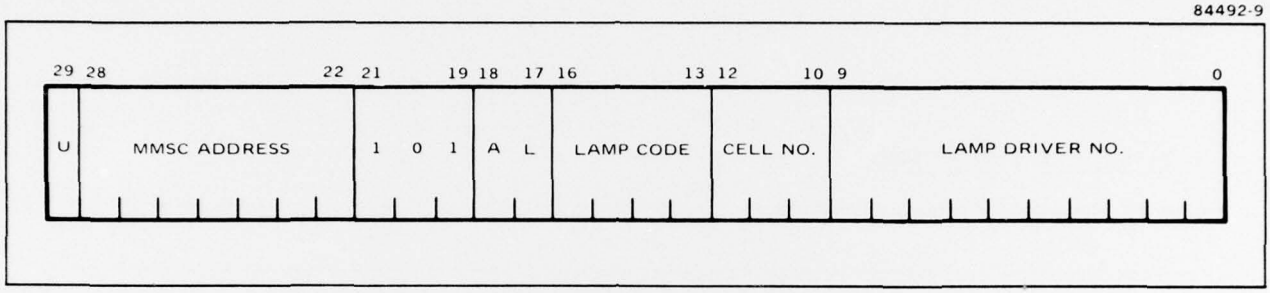
Memory Unload Stop

82492-4



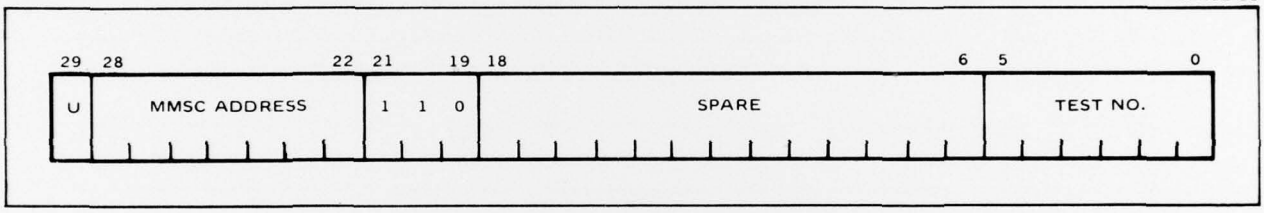
Passive-Format Word

84492-9



MMSC Indicator Word

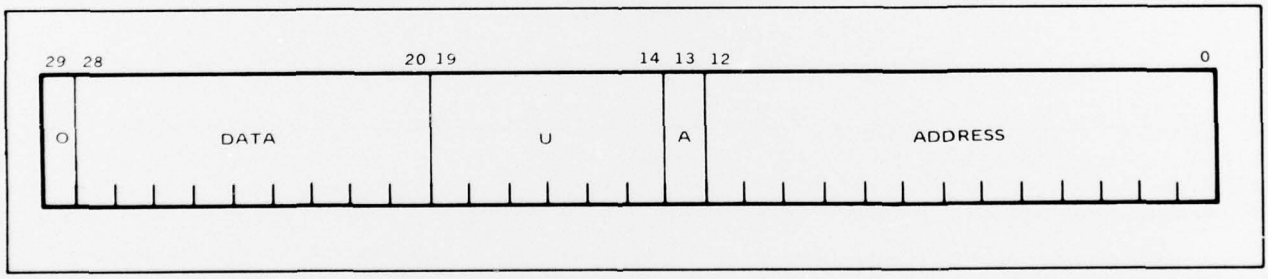
82492-11



Test Stimulus Word

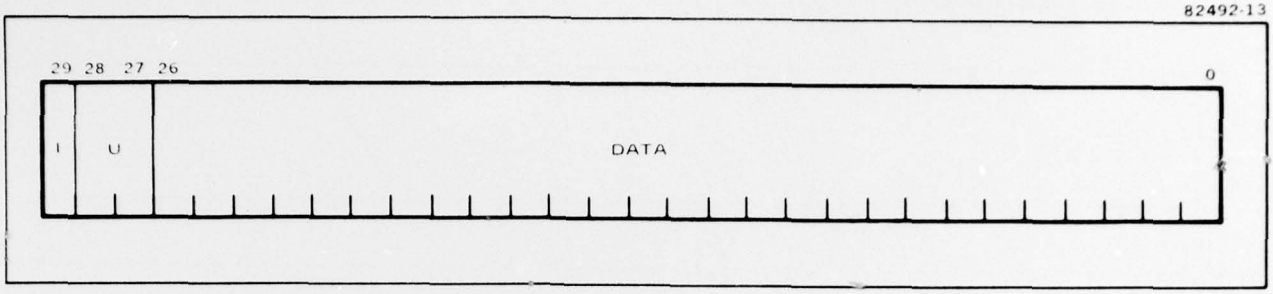
Output Acknowledge Words

82492-12



Word 1 of the Output Acknowledge Word Pair

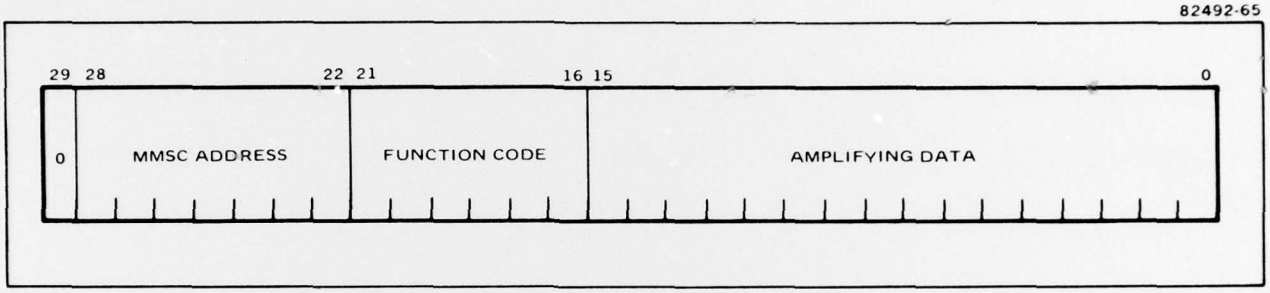
82492-13



Word 2 of the Output Acknowledge Word Pair

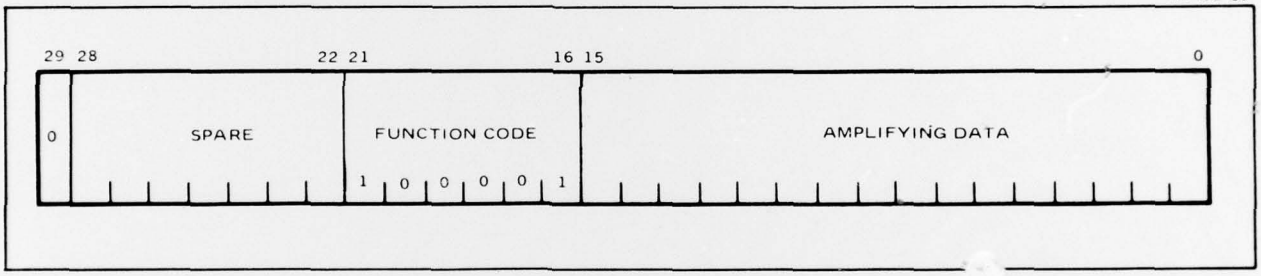
Interrupt Words

82492-65



MMSC

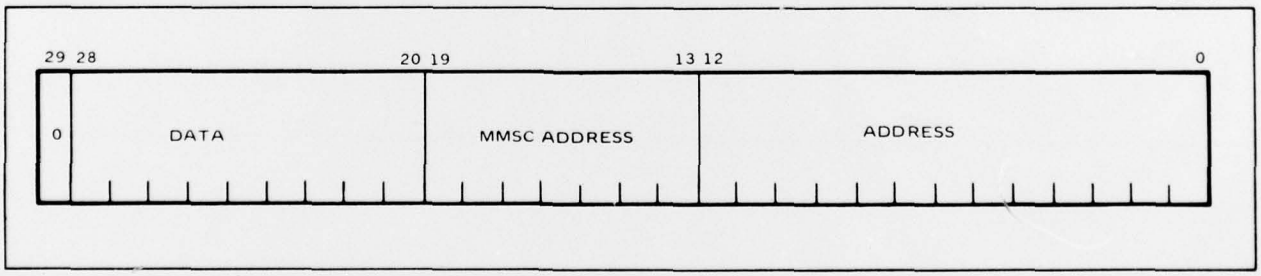
82492-67



PDMU

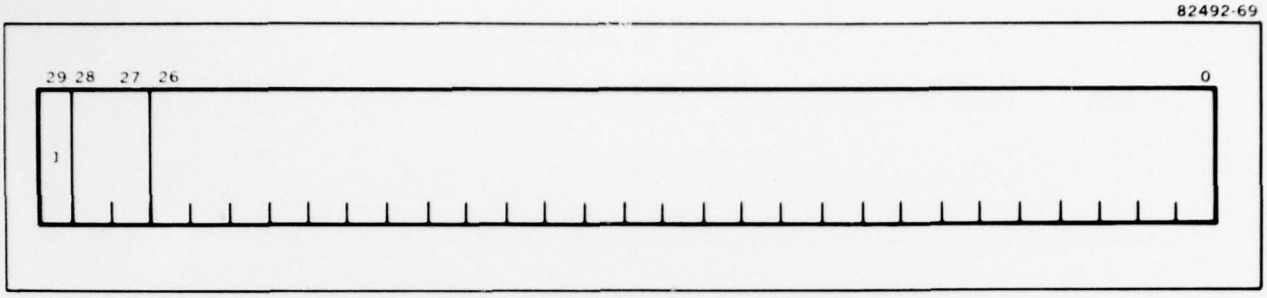
Input Data Request Words

82492-68



Word 1

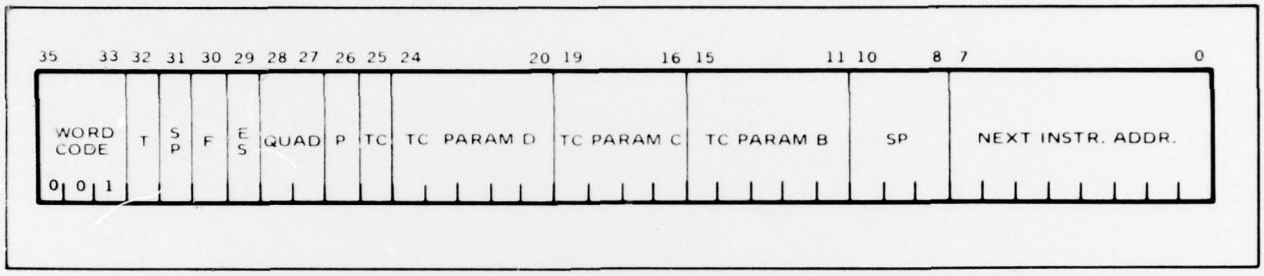
82492-69



Word 2

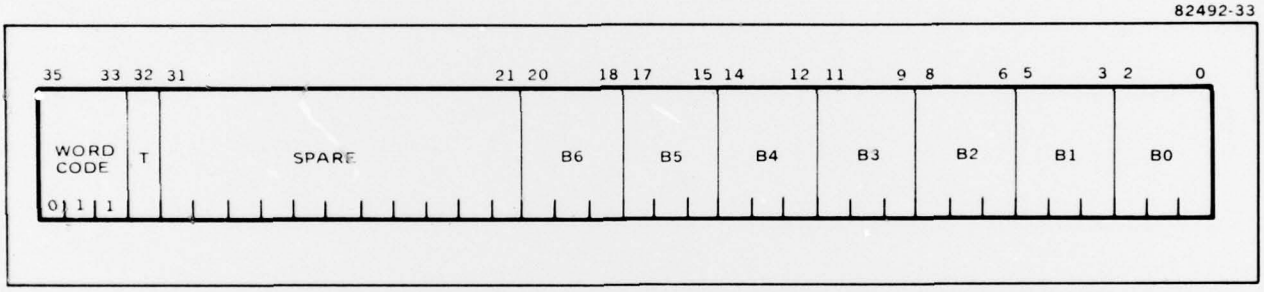
MMSC Instructions

82492-32



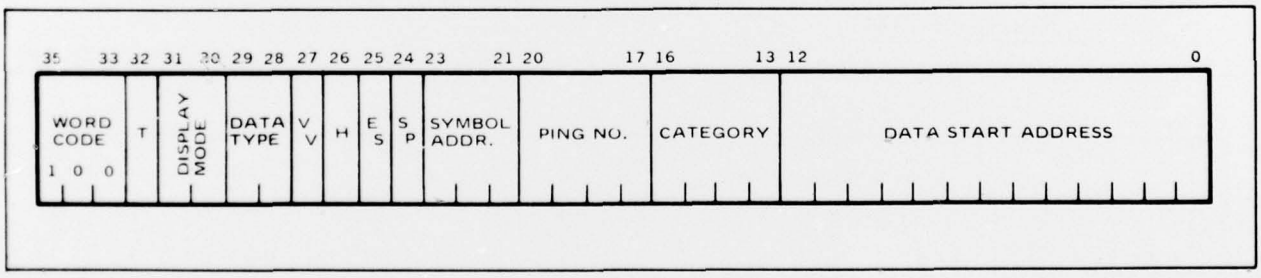
Format Control Word

82492-33



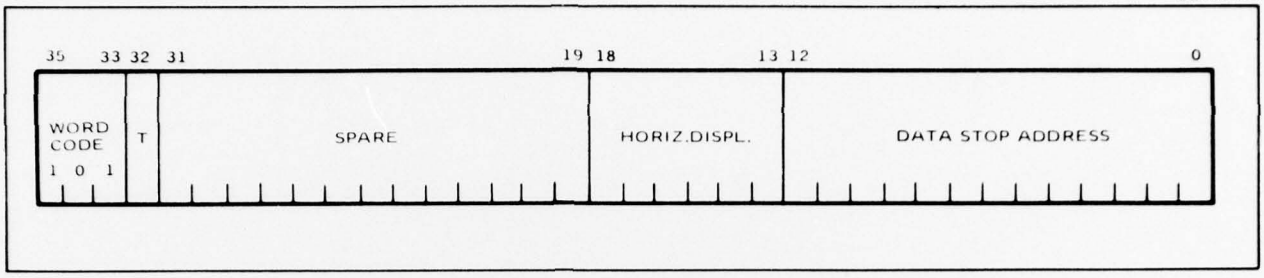
Time Compression Brightness Group Word

82492-34



Data Start Word

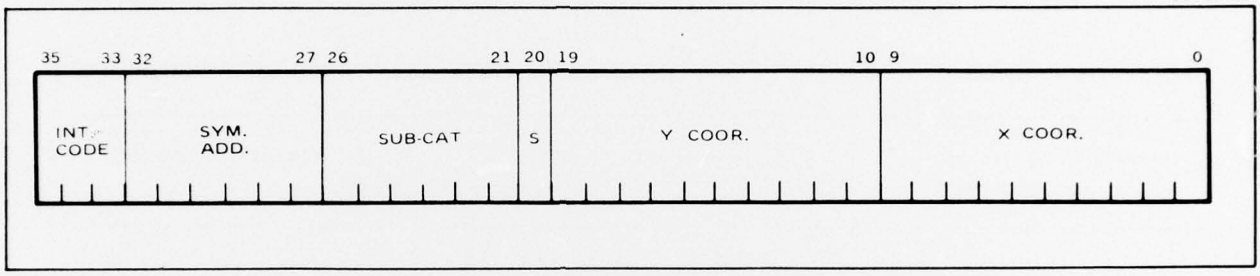
82492-35



Data Stop Word

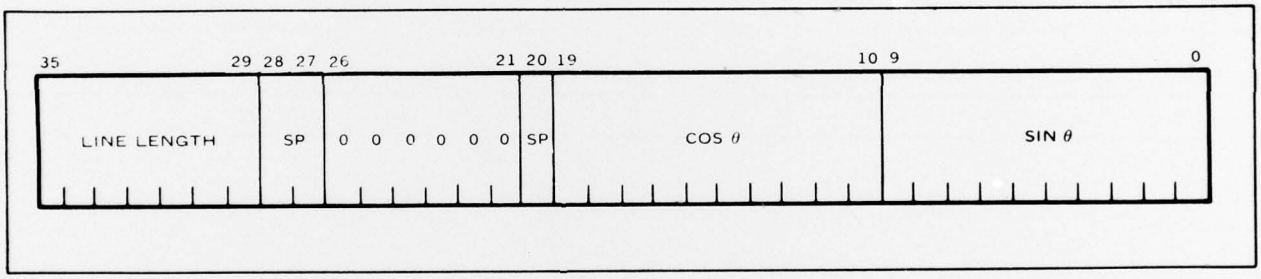
MMSC Data Words

82492-36



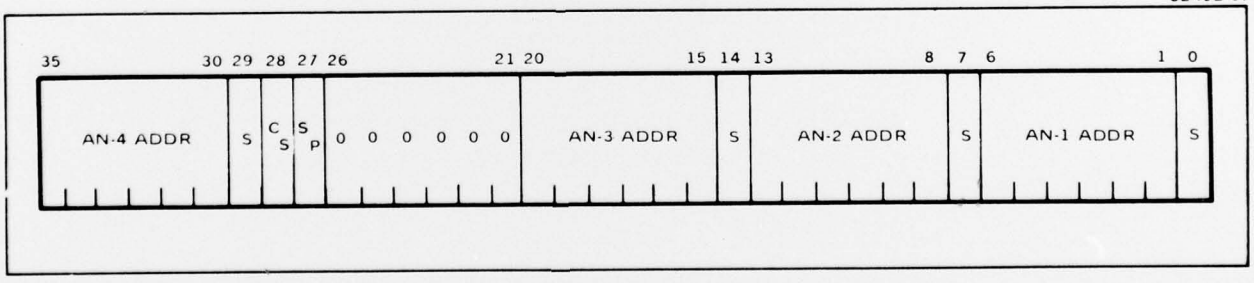
Position Word

82492-26



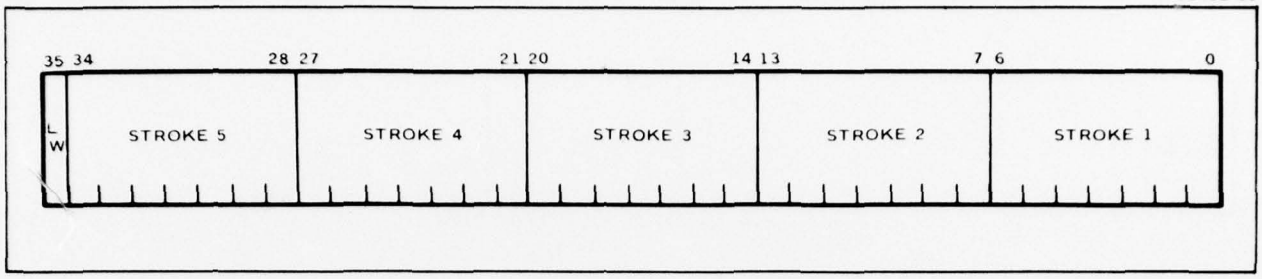
Line Word

82492-37



Alphanumeric Word

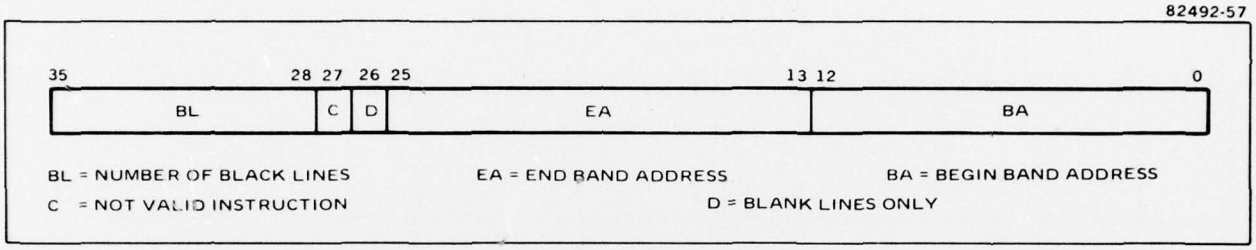
82492-38



Symbol Code Word

PDMU Instruction Word

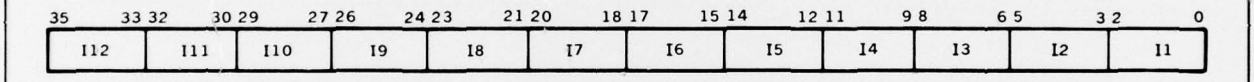
82492-57



PDMU Instruction Word

PDMU Intensity Word

82492-58



IN EACH INTENSITY FIELD, OCTAL CODING IS USED WITH THE LSB BEING THE LOWEST BIT NUMBER: THE OCTAL CODING IS AS FOLLOWS:

OCTAL CODE	INTENSITY MEANING
0	BLANK DISPLAY
1	INTENSITY LEVEL 1
2	INTENSITY LEVEL 2
3	INTENSITY LEVEL 3
4	INTENSITY LEVEL 4
5	INTENSITY LEVEL 5
6	INTENSITY LEVEL 6
7	INTENSITY LEVEL 7

PDMU Intensity Word